First Time, Every Time – Practical Tips for Phase-Locked Loop Design

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Outline

- Introduction
- Basic Feedback Loop Theory
- Jitter and Phase Noise
- Common Circuit Implementations
- Circuit Verification
- Design for Test

Introduction

How Are PLL's Used?

- Frequency Synthesis (e.g. generating a 1 GHz clock from a 100 MHz reference in a CPU)
- Skew Cancellation (e.g. phase-aligning an internal clock to the I/O clock) (May use a DLL instead)
- Extracting a clock from a random data stream (e.g. serial-link receiver)
- Reference Clean-Up (e.g. low-pass filter source-synchronous clock in high-speed I/O)

- ***Frequency Synthesis*** is the focus of this course.
- Design Priority? Frequency and/or phase accuracy?

What is a PLL?

- Negative feedback control system where f_{out} tracks f_{in} and rising edges of input clock align to rising edges of output clock
- Mathematical model of frequency synthesizer

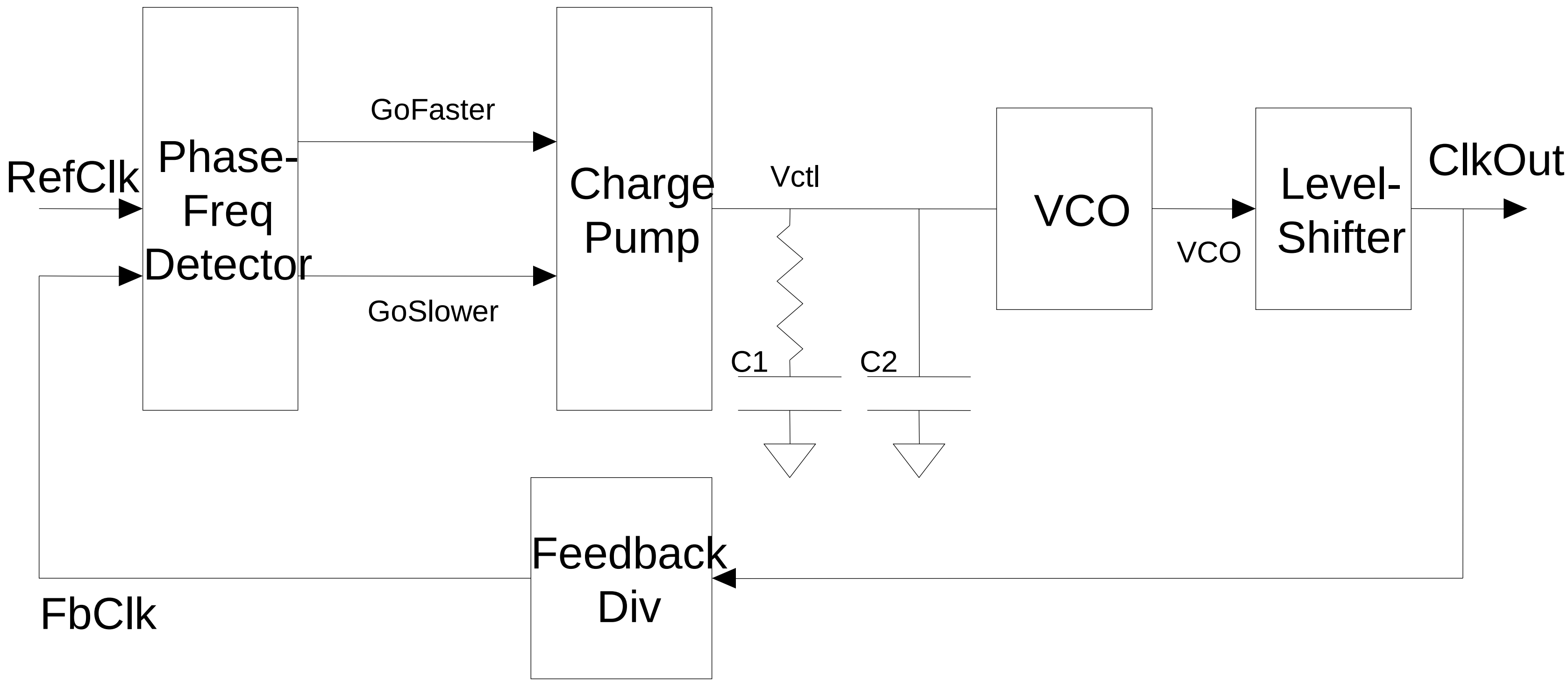
$$V_{in}(t) \propto \sin\overbrace{\left(2\pi f_{in} t\right)}^{\phi_{in}} \longrightarrow \boxed{\textbf{Phase-Locked Loop}} \longrightarrow V_{out}(t) \propto \sin\overbrace{\left(2\pi N f_{in} t\right)}^{\phi_{out}}$$

- **Phase = ∫ frequency**

$$\phi(t) = 2\pi \int f(t)\, dt \quad \leftrightarrow \quad f(t) = \frac{1}{2\pi}\frac{d\phi(t)}{dt}$$

- **When phase-locked,** $\phi_{out} = N\phi_{in} \rightarrow \; f_{out} = Nf_{in}$

Charge-Pump PLL Block Diagram



- Sampled-system (phase-error is input variable)
- Phase error is corrected by changing frequency ($\phi(t) = \int f(t)\, dt$)
- Resistor provides means to separate correction of frequency error from correction of phase error

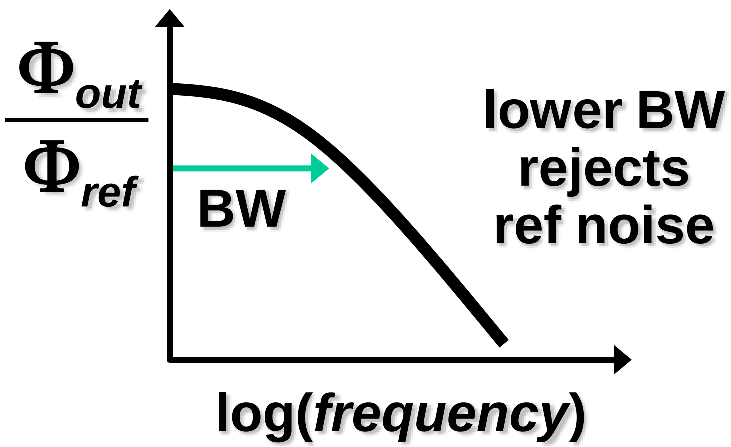
Components in a Nutshell

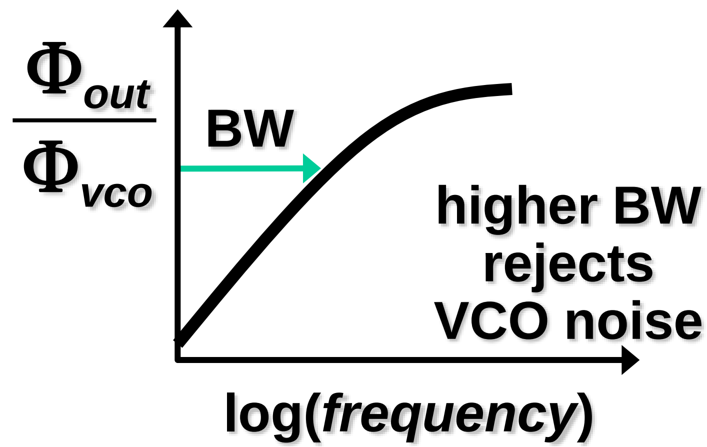
- Phase-Frequency Detector (PFD): outputs digital pulse whose width is proportional to sampled phase error
- Charge Pump (CP): converts digital error pulse to analog error current
- Loop Filter (LPF): integrates (and low-pass filters in continuous time) the error current to generate VCO control voltage
- VCO: low-swing oscillator with frequency proportional to control voltage
- Level Shifter (LS): amplifies VCO levels to full-swing
- Feedback Divider (FBDIV): divides VCO clock to generate FBCLK clock for phase comparison w/reference

PLL Feedback Loop Theory

What Does PLL Bandwidth Mean?

- PLL acts as a low-pass filter with respect to the reference modulation. High-frequency reference jitter is rejected
- Low-frequency reference modulation (e.g., spread-spectrum clocking) is passed to the VCO clock
- PLL acts as a high-pass filter with respect to VCO jitter
- “Bandwidth” is the modulation frequency at which the PLL begins to lose lock with the changing reference (-3dB)



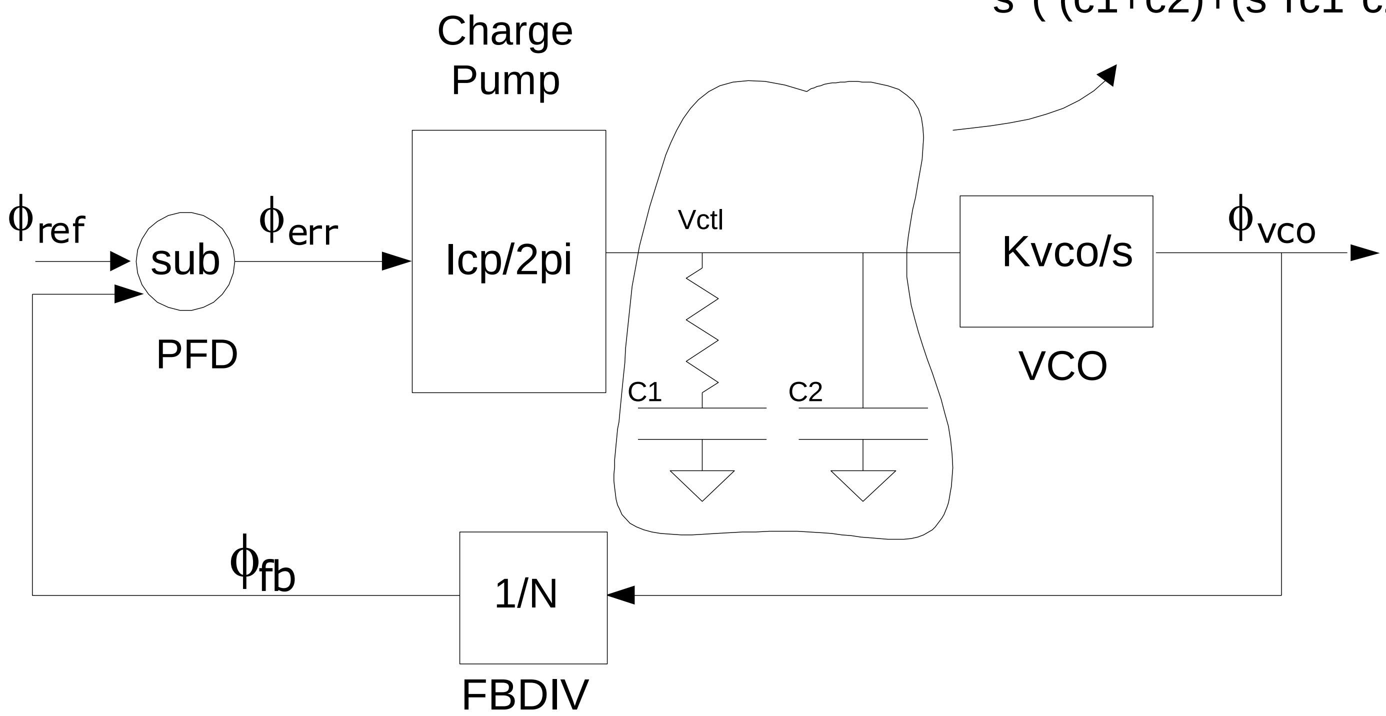


Closed-Loop PLL Transfer Function

- Transfer function describes how PLL responds to “excess” reference phase. i.e. RefClk phase modulation
- Analyze PLL feedback in frequency-domain
  - *Phase* is state variable, not frequency
  - “s” is the reference modulation frequency, not reference oscillation frequency
  - Assumes continuous-time (not sampled) behavior
- $H(s) = \phi_{fb}/\phi_{ref} = G(s)/(1+G(s))$ →closed-loop gain
- $G(s) = (K_{vco}/s)I_{cp}F(s)*e^{-sTd}/M$ → open-loop gain
  - where ϕ_{err}
    - K_{vco} = VCO gain in Hz/V
    - I_{cp} = charge pump current in Amps
    - F(s) = loop filter transfer function in Volt/Amp
    - M = feedback divisor
    - T_d = delay in feedback-loop (e.g. FBDIV, Tpfd/2)

PLL Components in Frequency Domain

$$Vctl(s) / Icp(s) = \frac{(1+s*rc1)}{s*(\ (c1+c2)+(s*rc1*c2)}$$



Closed-loop PLL Transfer Function

- $H(s) = \varpi_n^2\,(1+ s/\varpi_z) / (s^2+2s\zeta\varpi_n + \varpi_n^2)$
  - where
    - ϖ_n = undamped natural frequency (rad/s)
    - ϖ_z = stabilizing zero = $1 /RC_1$ (rad/s)
    - ζ = damping factor
  - 2^{nd}-order (two poles p1,p2 and one zero)
  - 2^{nd}-order ignores C_2 cap and feedback delays

- If $\zeta < 1$, complex poles lead to damped oscillation
  - Real → exponential decay($\zeta\varpi_n$) , Imag → oscillation (ϖ_n)

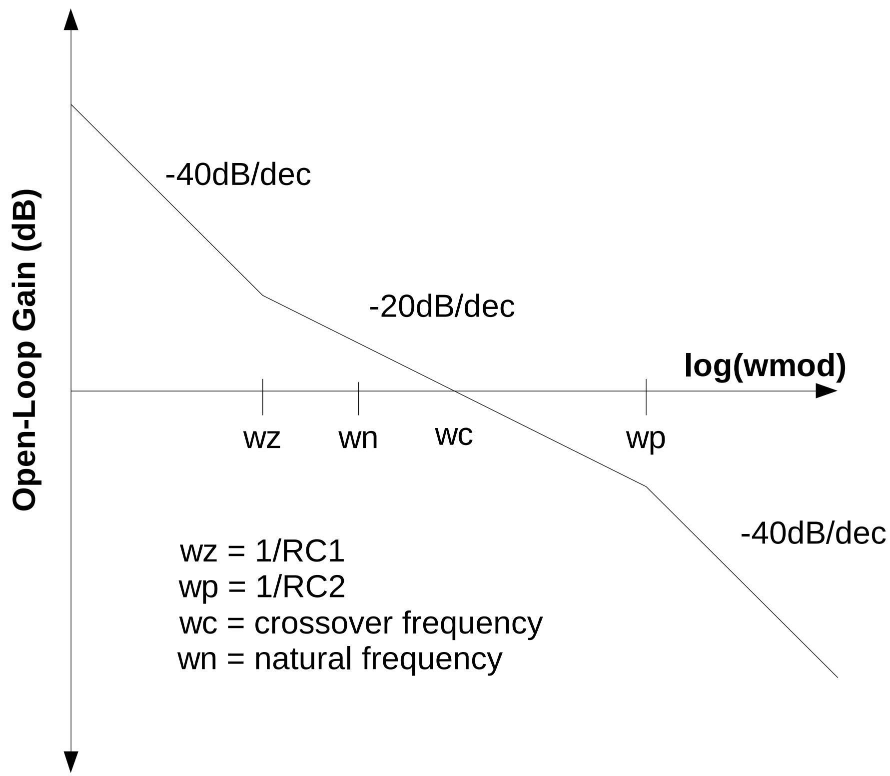
- If $\zeta > 1$, z and p1 cancel: BW(-3dB) ~ $2s\zeta\varpi_n$

What is a “Zero”?

- The “Zero” of the closed-loop transfer function is the frequency in radians/s where the gain of the integral and proportional paths are equal.
- Classic loop: $\varpi_z = 1 / RC_1$ (rad/s)
- Concept can be applied to loop filters that do not contain a resistor.

Open-Loop Transfer Function

- log(Gain) vs. log(Modulation Frequency)
- 2 poles @ origin, 1 zero @ wz, 1 pole @wp



Bandwidth

- Undamped Natural Frequency:
  - ϖ_n = sqrt(K_{vco}*I_{cp}/(M*C_1)) in rad/sec
  - where
    - K_{vco} = VCO gain in **Hz/V**
    - I_{cp} = charge pump current in Amps
    - M = feedback divisor
    - C_1 = large LPF capacitor

- For stability: $\varpi_n/2\pi$ < ~1/15 reference frequency
- Typical value: 500 kHz < $\varpi_n/2\pi$ < 10MHz

Stability, Damping, and Phase Margin

- Damping Factor: $\zeta = R_{lpf} * C_1 * \varpi_n /2$
  - Dimensionless, Usually $\sim 0.45 < \zeta < \sim 2$
  - Lower end of range for low period jitter
  - Higher end of range for accurate ref phase tracking
  - R_{lpf} provides means to set stability independent of bandwidth

- ϕ_m (degrees) = $(180/\pi)*(\mathrm{atan}(\varpi_c*RC_1) - \mathrm{atan}(\varpi_c*RC_2) - \varpi_c*T_{dly})$
  - ϖ_c == crossover frequency
    - frequency where open-loop gain G(s) = 0dB
  - For stability: $1/RC_1$ (zero) $< \varpi_c < 1/RC_2$ (parasitic pole)
  - Typical Range: $1.2*\varpi_n < \varpi_c < 2.5*\varpi_n$

- Phase margin degradation due to PFD phase error sampling
  - $-\phi = \varpi_c * T_{ref} / 2$
  - z-domain analysis is more accurate

- Phase margin (ϕ_m) ~ 100 * ζ (for $\zeta < 0.5$)
  - Usually 45° < PM < 70°

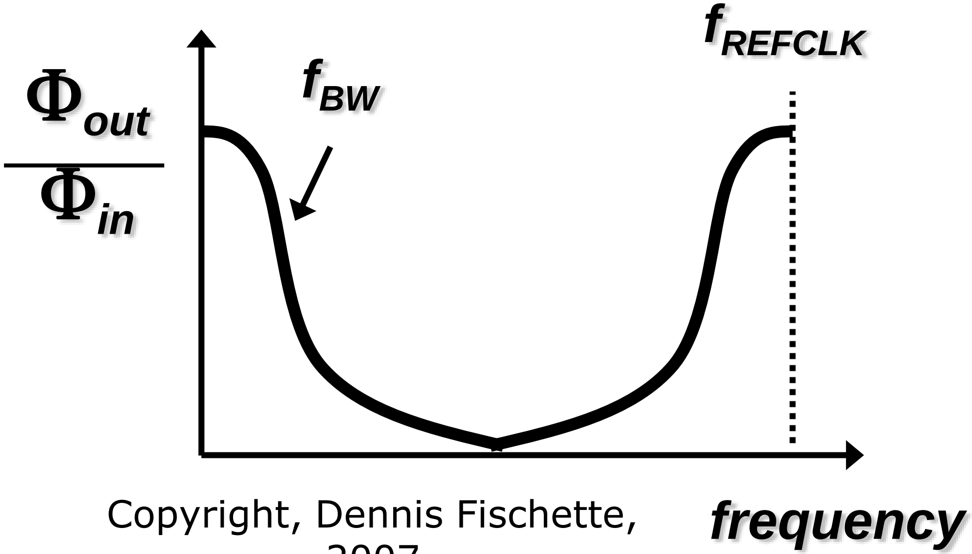
Loop Dynamics vs. OSR

- Assumes continuous-time model. Damping = 0.8, wn = 3.7MHz
- ϕ_m=62° , BW(-3dB)=8.8MHz, Pk=2.1dB (w/no delay)

OSR (wn(Hz)/f(ref)	Phase Margin(°)	Peaking(dB)	BW(-3dB) (MHz)
4.5	-4	26	10.6
6.7	18	11	12.6
7.6	24	8.0	13.1
8.9	29	6.0	13.4
10.7	35	4.6	13.5
13.3	40	3.6	13.1
17.8	46	3.0	12.1
26.7	51	2.6	10.9
53.4	56	2.3	9.1

Aliasing in a Sampled Loop

- Sampling nature of PFD → frequency-domain aliasing
  - Can't low-pass filter ref noise before PFD sampling – unlike A/D's
  - Need z-domain analysis for accurate PLL modeling – analogous to sample-and-hold
- Phase of modulation with respect to ref affects aliasing
  - e.g. ref modulation at ½ * f_{ref}. No jitter if sampled at 0°,180°, max at 90°,270°
- Modulation at frequencies > Nyquist ($f_{ref}/2$) appears at other frequencies
  - e.g. f_{ref}=100MHz → ref modulation at 99MHz looks just like 1MHz ref modulation to the PLL
  - continuous-time model says that PLL should reject more 99MHz noise than 1 MHz noise



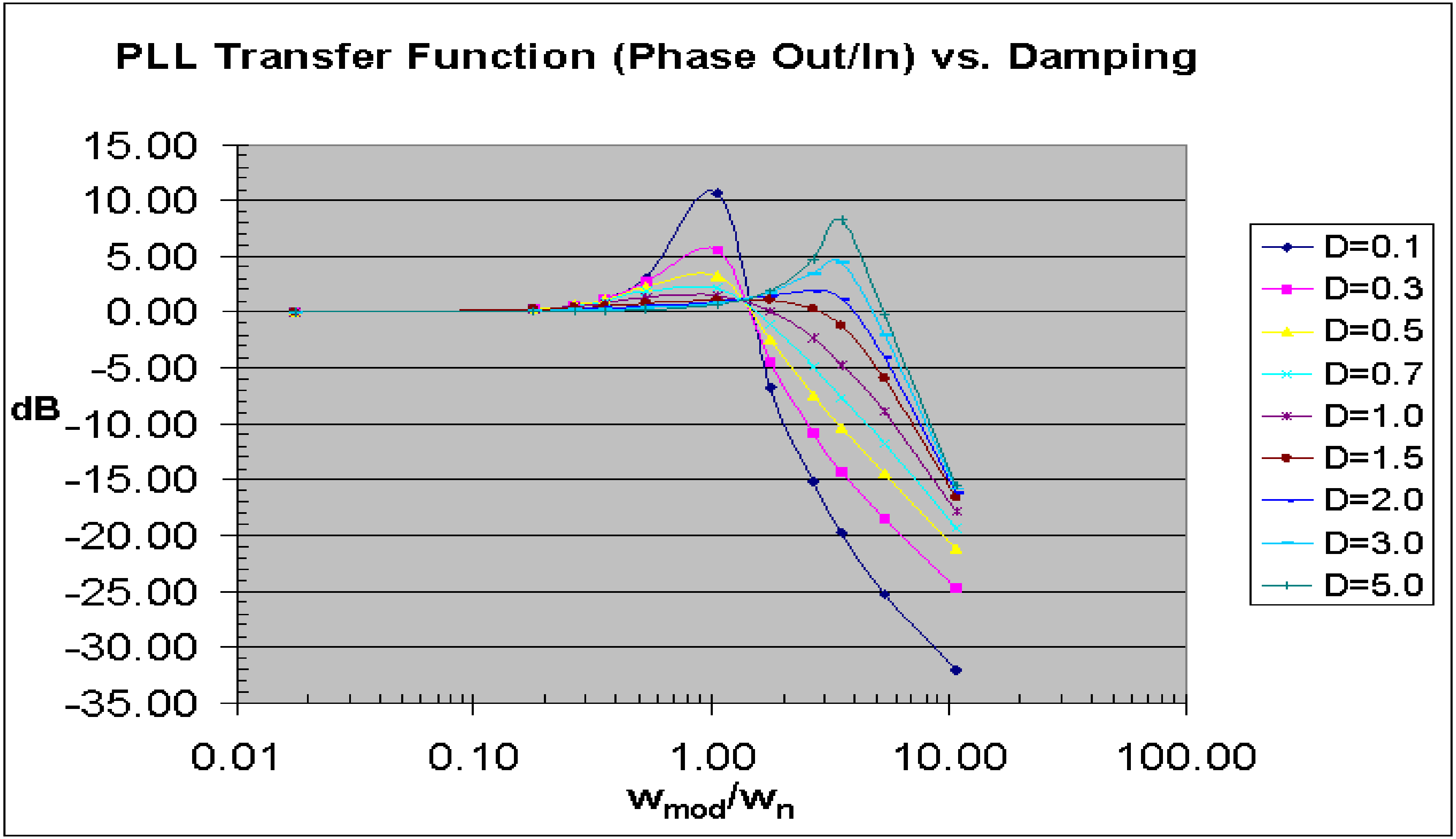
PLL Response vs. Damping

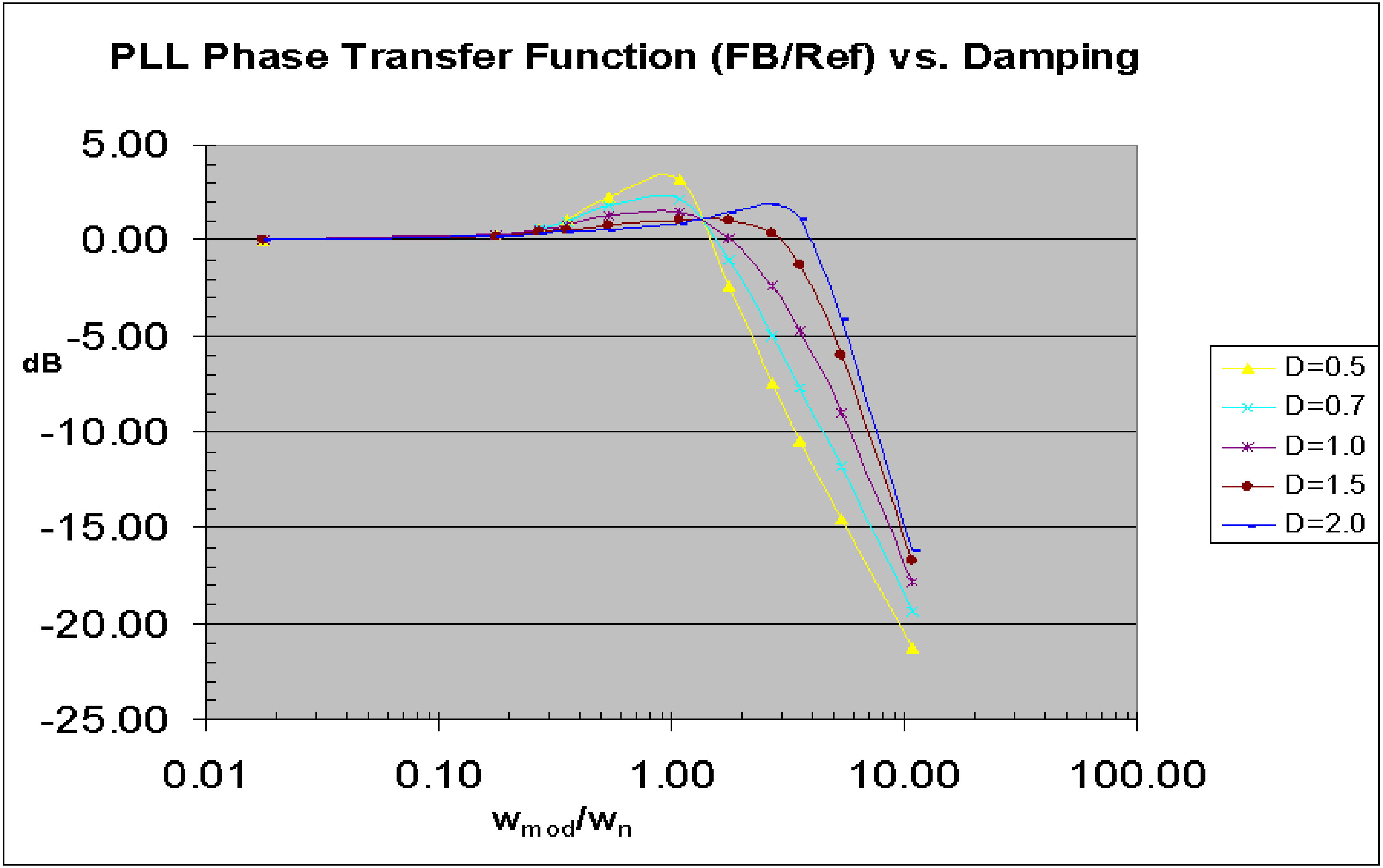
Phase Tracking vs. Damping

- Phase Tracking vs. Damping
- Closed-loop Transfer Function (ϕ_{fb}/ϕ_{ref})
- Phase Tracking → think "accumulated" period jitter or phase error
- Peaking at low and high damping factors → bad
- Peaking at high damping due to smoothing capacitor pole ($1/RC_2$) and/or under-sampling (Gardner)
- Peaking very sensitive to ($1/RC_2$) at high R
- Min peaking w/damping ~ 1.0 - 1.5 if C_2 ~ 5% * C_1
- Typical peaking: 1 – 3 dB (CPU high-end, IO low-end)
- For lower peaking, damping > 2 and C_2 small

- Simulation Condition (following slides): C_2 = 6.7% * C_1

Closed-loop Transfer Function

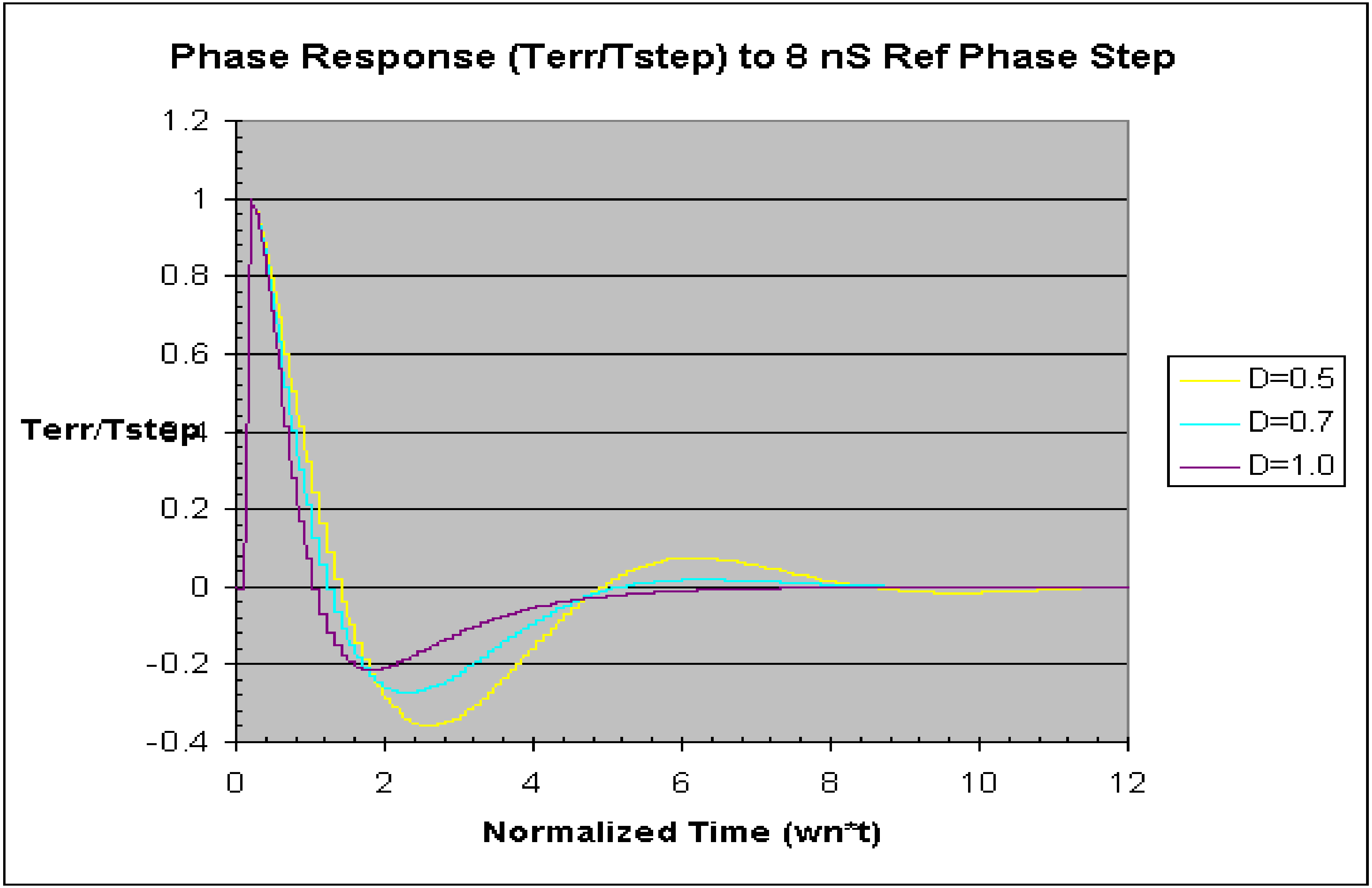



PLL Phase Transfer Function (FB/Ref) vs. Damping
5.00
0.00
-5.00
-10.00
-15.00
-20.00
-25.00
dB
0.01
0.10
1.00
10.00
100.00
w_{mod}/w_n
D=0.5
D=0.7
D=1.0
D=1.5
D=2.0

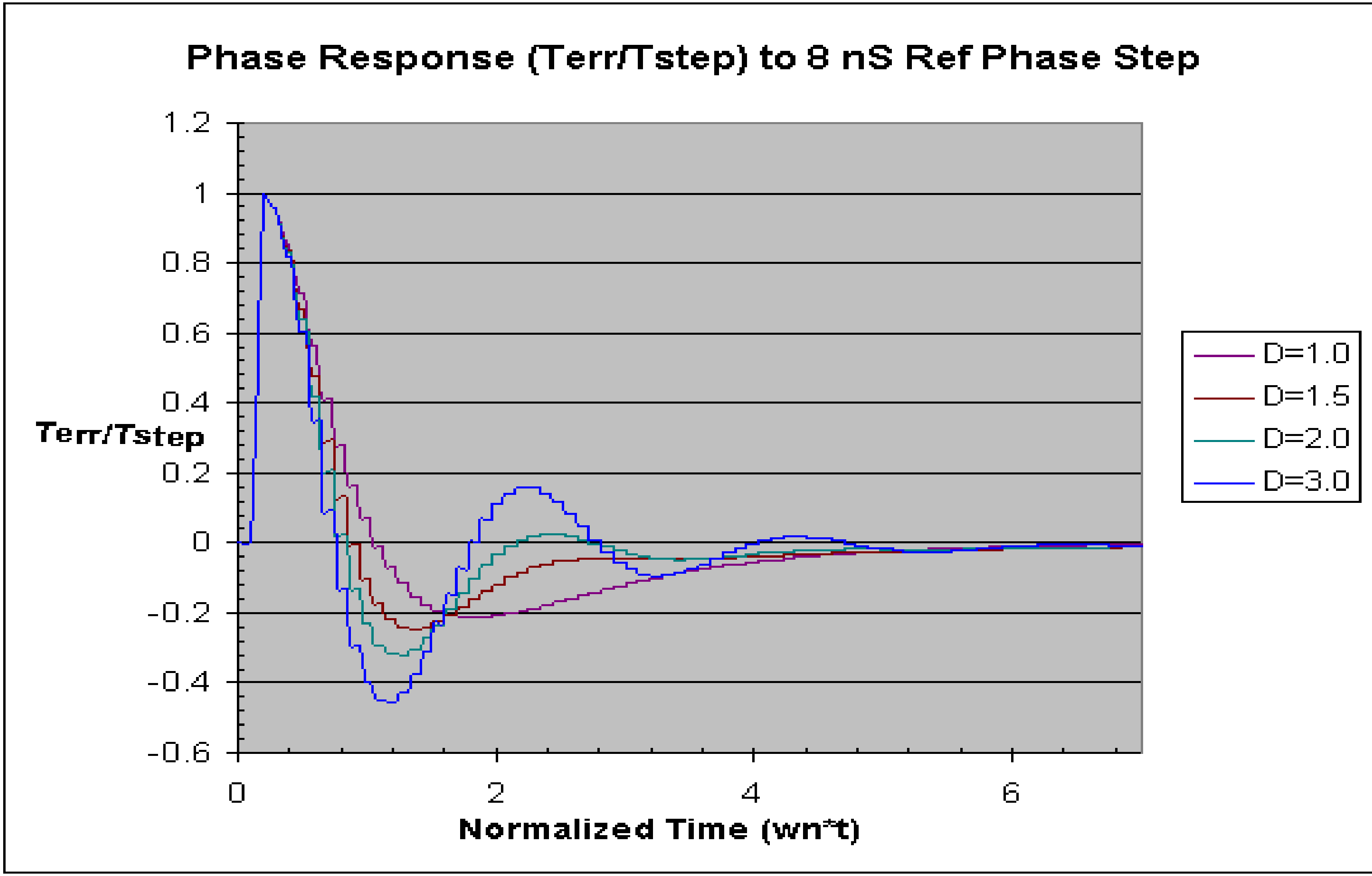
Phase Response vs. Damping (time-domain)

- Transient Simulation Conditions (behavioral model):
  - step reference phase by 2π radians. Observe phase overshoot
  - $C_2 = 10\% * C_1$ (high end of C_2 range requires lower ζ)

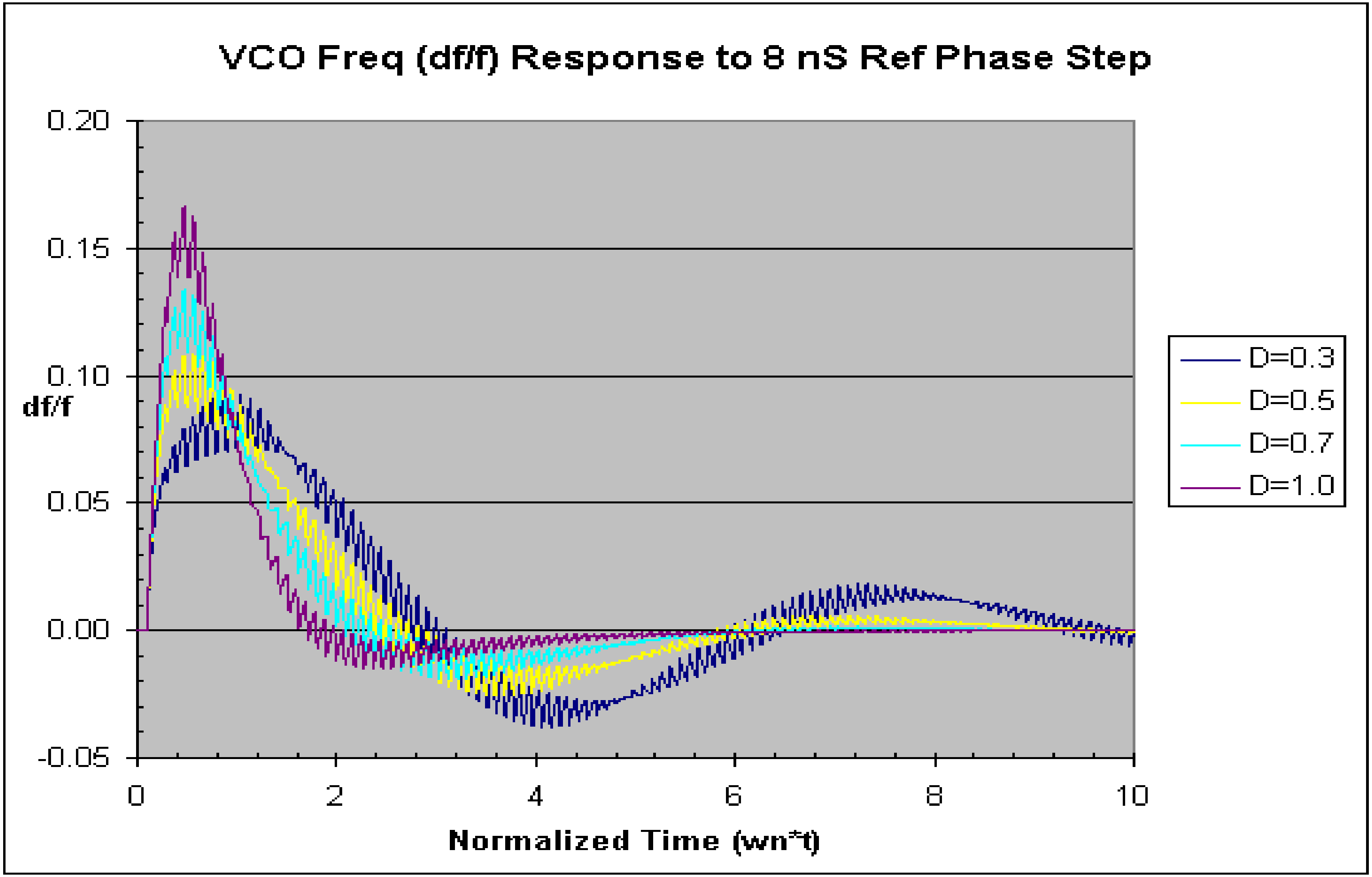
- Less ringing and overshoot as $\zeta \rightarrow 1$
- Severe under-damping → slow ringing and overshoot
- Severe over-damping → fast ringing and overshoot
- Ringing at high damping due to smoothing pole (large RC_2) and/or low over-sampling

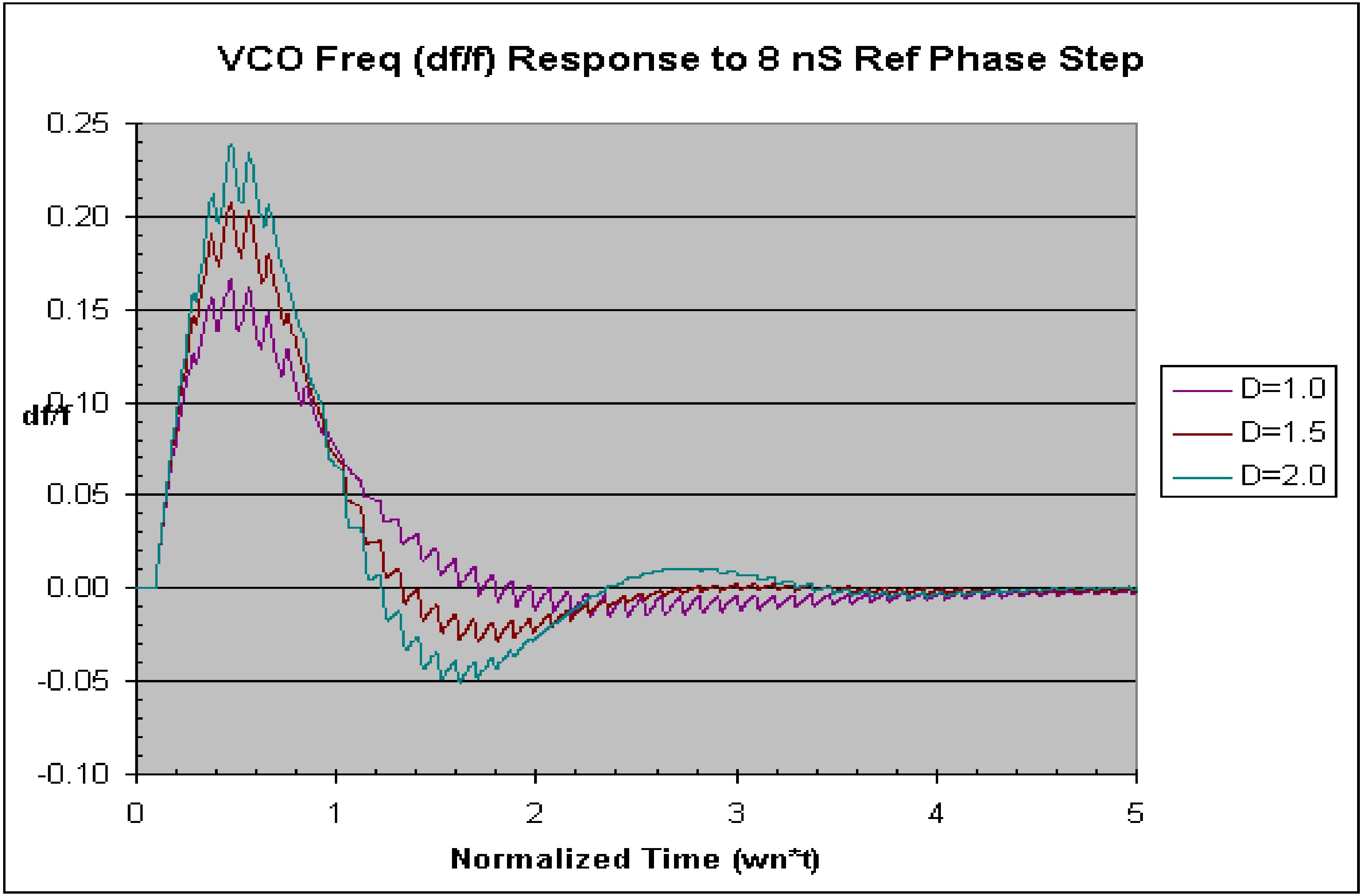


Phase Response (Terr/Tstep) to 8 nS Ref Phase Step
Terr/Tstep
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
0
2
4
6
8
10
12
Normalized Time (wn*t)
D=0.5
D=0.7
D=1.0


Phase Response (Terr/Tstep) to 8 nS Ref Phase Step
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
Terr/Tstep
0
2
4
6
Normalized Time (wn*t)
D=1.0
D=1.5
D=2.0
D=3.0

Frequency Response vs. Damping




VCO Freq (df/f) Response to 8 nS Ref Phase Step
0.25
0.20
0.15
0.10
df/f
0.05
0.00
-0.05
-0.10
0
1
2
3
4
5
Normalized Time (wn*t)
D=1.0
D=1.5
D=2.0

Jitter and Phase Noise

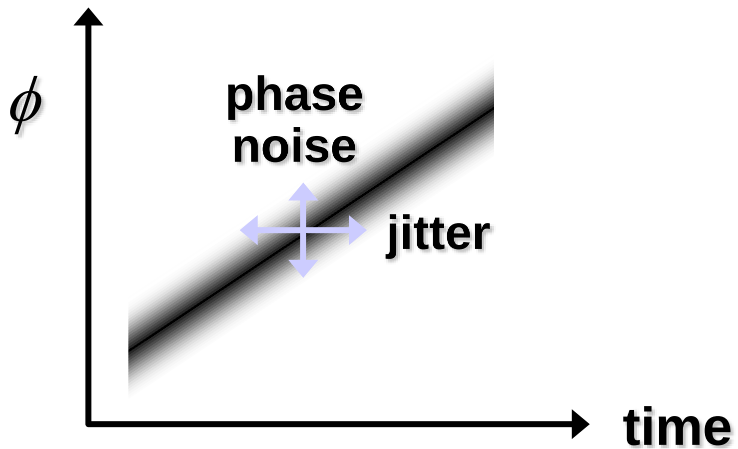
Phase Noise and Timing Jitter

- **Phase Noise (frequency domain) ↔ Jitter (time domain)**
- **Noise is frequency-dependent with random & deterministic components**

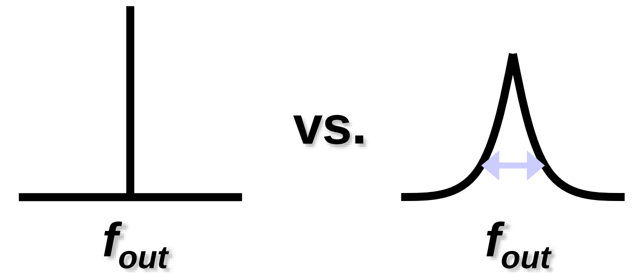
- **VCO and loop filter resistor often largest sources of noise**

PLL Output

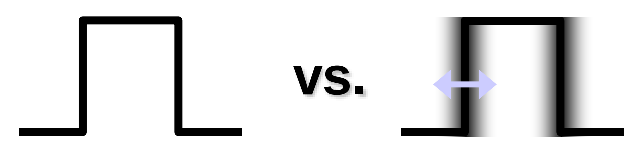
$$V_{out}(t) \propto \sin\left(2\pi f_{out} t + \phi_n(t)\right)$$



Frequency Domain

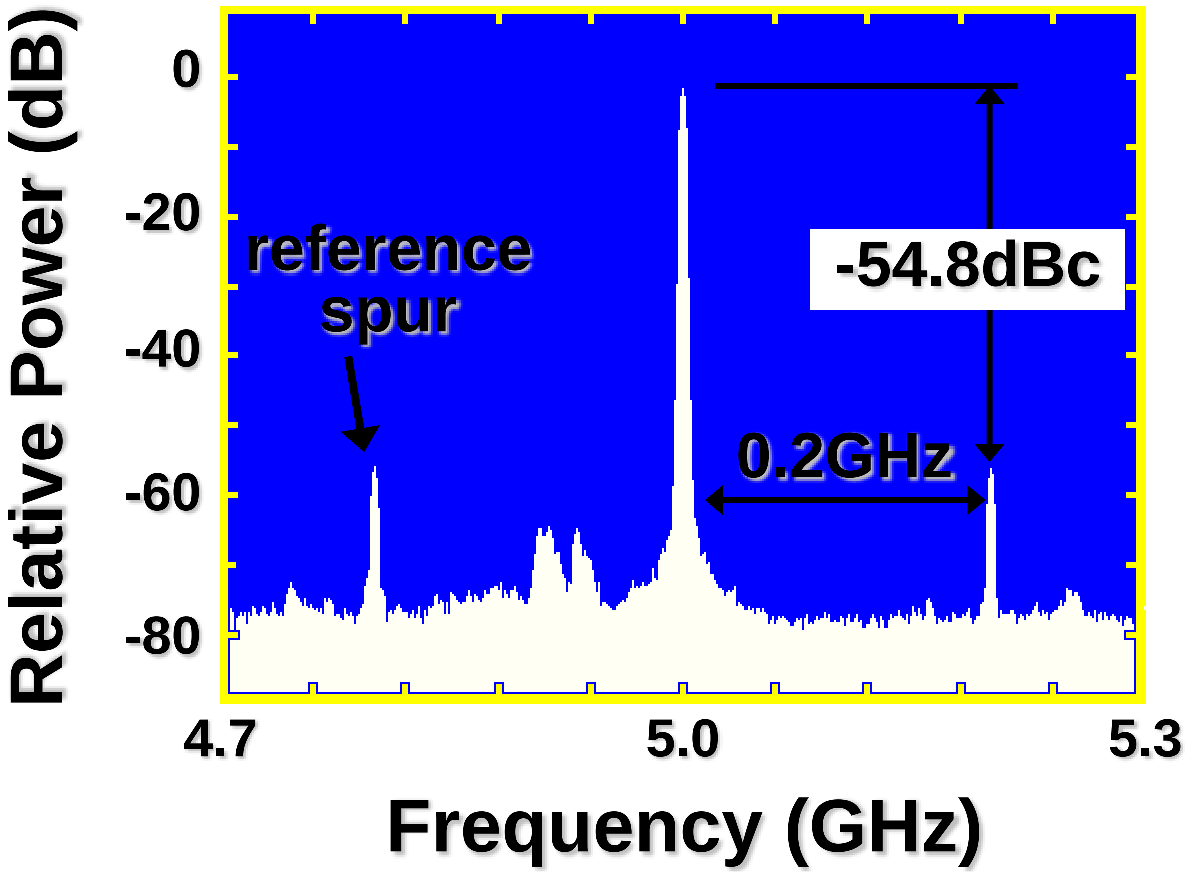


Time Domain



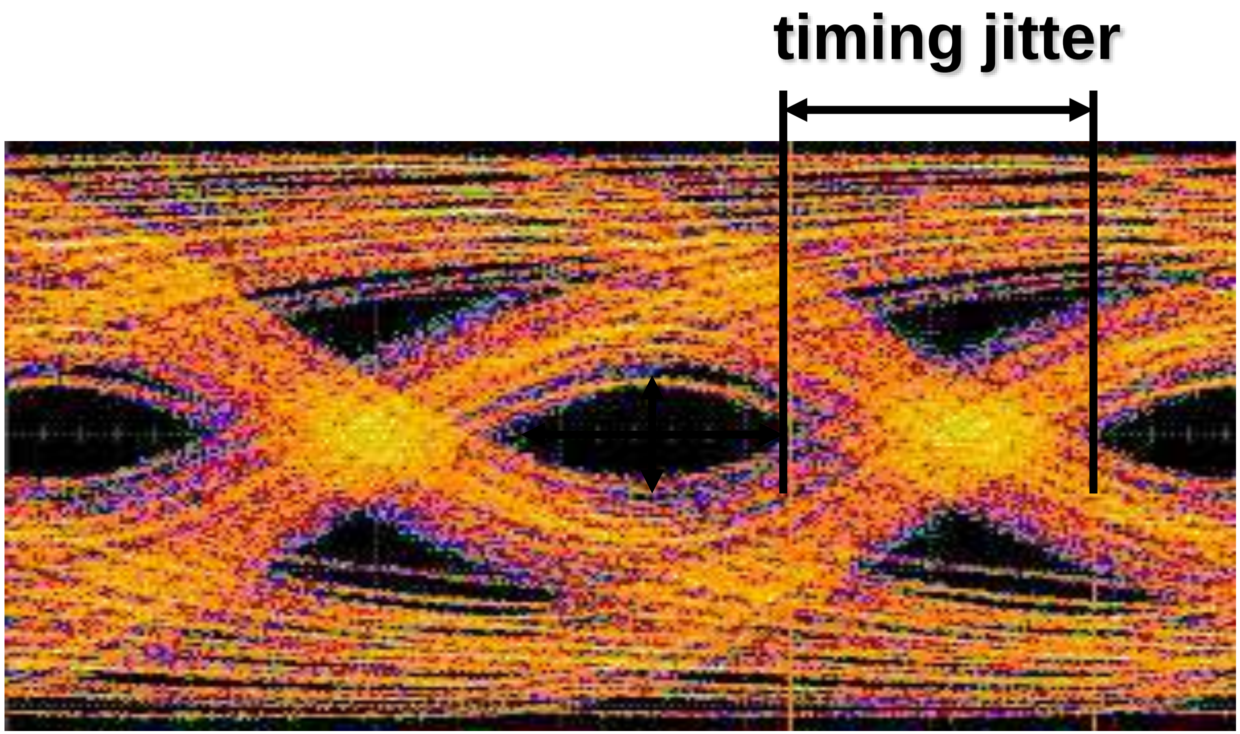
Spectral Analysis of VCO Clock

- 5GHz VCO clock with 200MHz reference clock



Timing Jitter: Eye Diagram

- Example of timing jitter in serial link.
- Overlay scope traces of several bits on top of each other



Jitter Definitions

- Phase Jitter (sec)
  - deviation of VCO output edges from ideal placement in time.
  - specified over a time interval or frequency range.
  - important for I/O apps (e.g. PCI-Express < ±1.5ps RMS)
  - measure with spectrum analyzer or scope with jitter package
- Period Jitter (sec)
  - deviation of VCO period from ideal period
  - derivative of Phase Jitter with respect to time
  - peak-to-peak period jitter (J_{pp}) is max VCO period – min VCO period
  - most important for CPU-like apps
  - e.g. 10-20ps for 2GHz CPU clock
  - easily measured on scope – self-triggered infinite-persistence or jitter package
- Cycle-to-Cycle Jitter (sec)
  - change in VCO period from cycle N to cycle N+1
  - derivative of Period Jitter with respect to time
  - not important for CPU-like apps

Jitter Definitions

- TIE (sec)
  - time difference between total of N-consecutive actual VCO cycles and N ideal cycles
  - easily measured on oscilloscope with jitter package – self-triggered measurement
  - TIE – “time-interval error”

Noise Sources

- Major internal PLL Noise Sources
  - charge-pump (flicker (1/f) and thermal)
  - loop filter resistor (thermal) – very significant
  - VCO (mostly thermal) - significant
  - VCO bias (flicker and thermal) – most significant
  - Flicker Noise
    - V_n^2 (V^2/Hz) = K_f / (C_{ox}*W*L* f)
    - $K_f \sim 10e^{-24}$
  - Thermal Noise
    - I_n^2 (Amp^2/Hz) = 4kT*g_m*γ
    - $\gamma \sim 2/3$ for older CMOS technologies, much higher in deep submicron
- PLL feedback loop
  - Low-pass filters ref and charge-pump noise
  - Band-pass filters loop-filter resistor noise
  - High-pass filters VCO noise (1-H(s))

Output Phase Noise

- Measured vs. offset frequency (f) from carrier

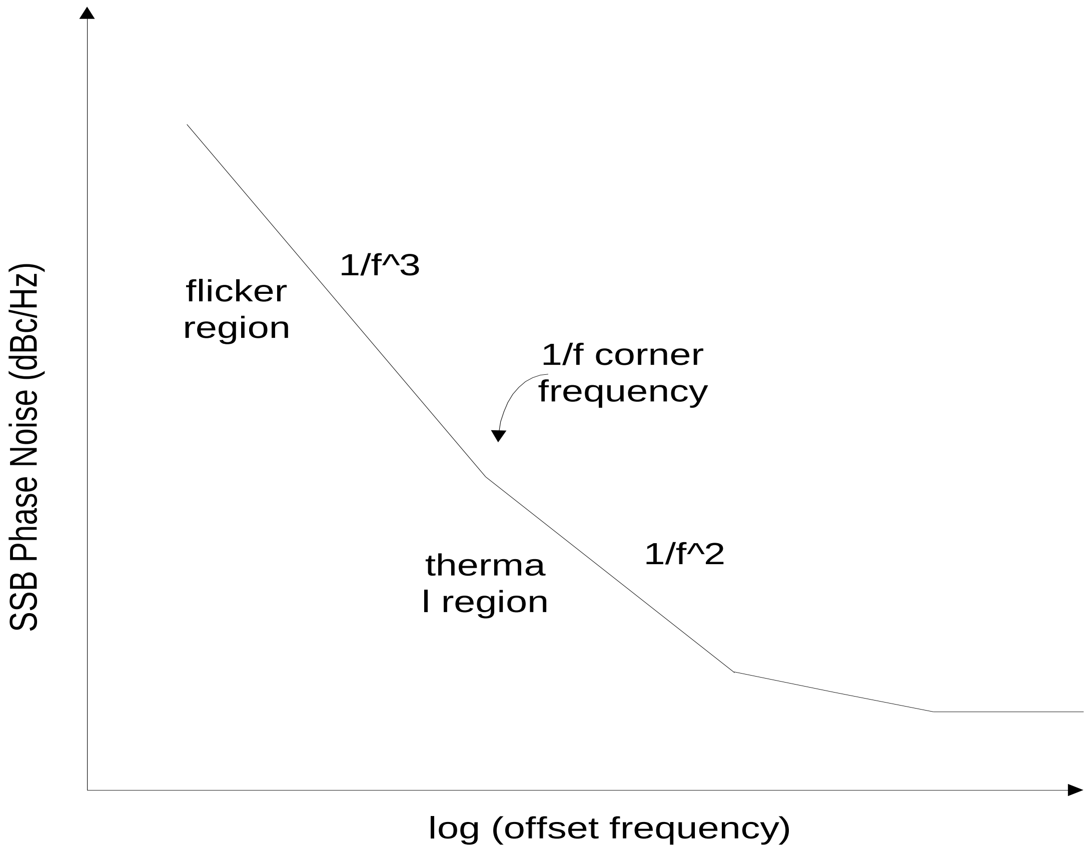
- Spectral Density of Phase Fluctuations ($S\phi(f)$)
  - $S\phi(f) = 2L(f)$
    - $L(f)$ is Single-Sideband Phase Noise
  - Analogous to Power(sideband)/Power(carrier)
  - $S\phi(f)$ is specified in a 1Hz band

- $S\phi(f) \sim 1 / f^2$ (thermal region, mid-to-high f) (open-loop)
- $S\phi(f) \sim 1 / f^3$ (flicker region, low f) (open-loop)

- Flicker noise mostly filtered by high BW PLL

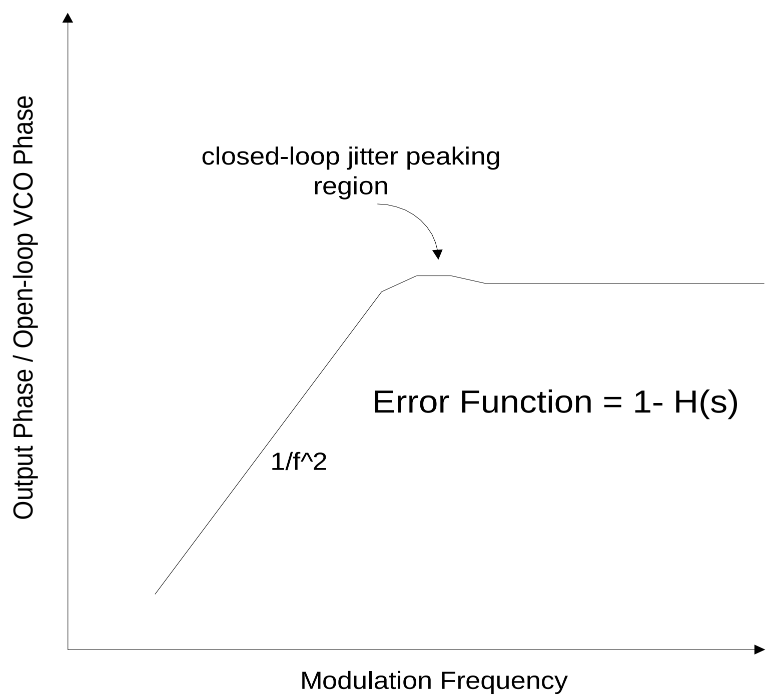
Single-Sideband Phase Noise Plot

- Open-loop VCO



Open-loop → Closed-Loop Phase Noise

- Goal: determine how much open-loop VCO phase noise remains after applying PLL feedback loop
- Method: multiply VCO's open-loop single-sideband phase noise by PLL's "error function" (1- H(s)) where H(s) is closed-loop transfer function



Converting Phase Noise to Jitter

- RMS Phase Jitter

$$J_{phase} = \frac{1}{2\pi f_{vco}} \sqrt{\int S_{\phi}(f)\,df}$$

- Usually dominated by VCO bias and loop filter
- Easily measured using spectrum analyzer – low noise floor
- Ideal reference is measurement trigger
- Integration range depends on application (e.g., PCIe: f_{min}= 1.5MHz)
  - usually stop integration at $f_0/2$ to avoid capturing carrier and harmonics
  - e.g., 5ps from 1MHz to $f_0/2$ with BW=15MHz and 2.5GHz clock (SOI bad for phase jitter)

Converting Phase Noise to Jitter

- RMS Period Jitter

$$J_{period} = \frac{1}{2\pi f_{vco}} \sqrt{8 \int L(f) \sin^2\left(\frac{\pi f}{f_{vco}}\right) df}$$

- Spectrum analyzer can't do this integral. Post-process phase noise
  - e.g., J_{per}~300fs w/2.5GHz clock
- Usually dominated by VCO bias and VCO?
- Spectrum analyzer usually has lower noise floor than scope (scope floor ~800fs @ 40Gsample/sec)

Converting Phase Noise to TIE

- Time-Interval Error (TIE)

$$J_{TIE} = \frac{1}{2\pi f_{vco}} \sqrt{8\int L(f)\sin^2(\pi f\tau)df}$$

- "Tau" is time interval over which phase drift is measured
- Spectrum analyzer can't do this integral. Post-process phase noise

VCO Noise Tracking: Phase Error vs. Bandwidth

- For random VCO noise (i.e. thermal):
- lower BW → more accumulated phase error
- Why? More jittery VCO cycles before feedback can correct:

$$\phi_{error} \propto J_{RMS,period} \cdot \sqrt{\frac{\omega_{vco}}{\zeta\omega_n}}$$

where J_{rms} = VCO RMS period jitter

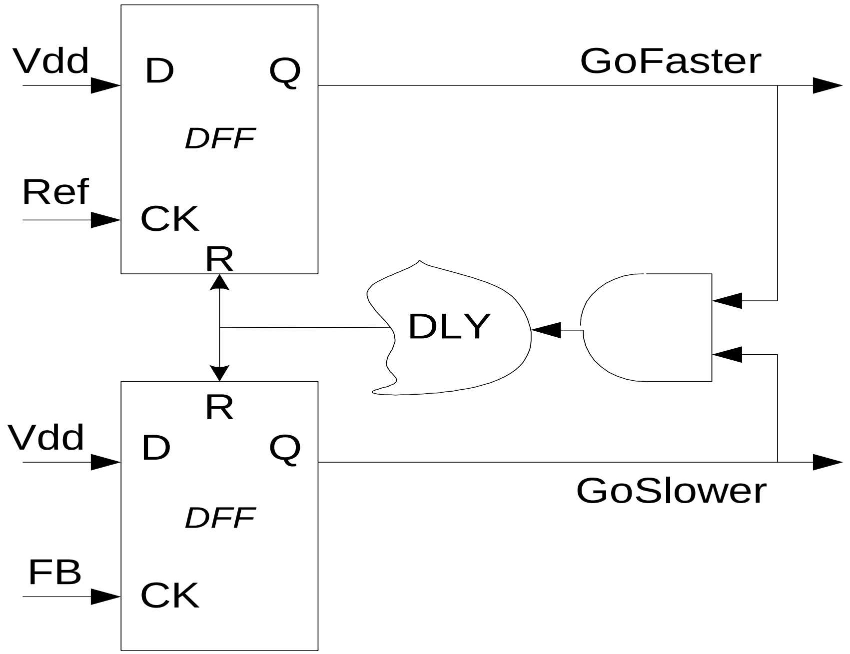
PLL Circuits

- Phase-Frequency Detector
- Charge-Pump
- Loop Filter
- Voltage-Controlled Oscillator
- Level-Shifter
- Feedback Divider
- Voltage Regulator
- Miscellaneous

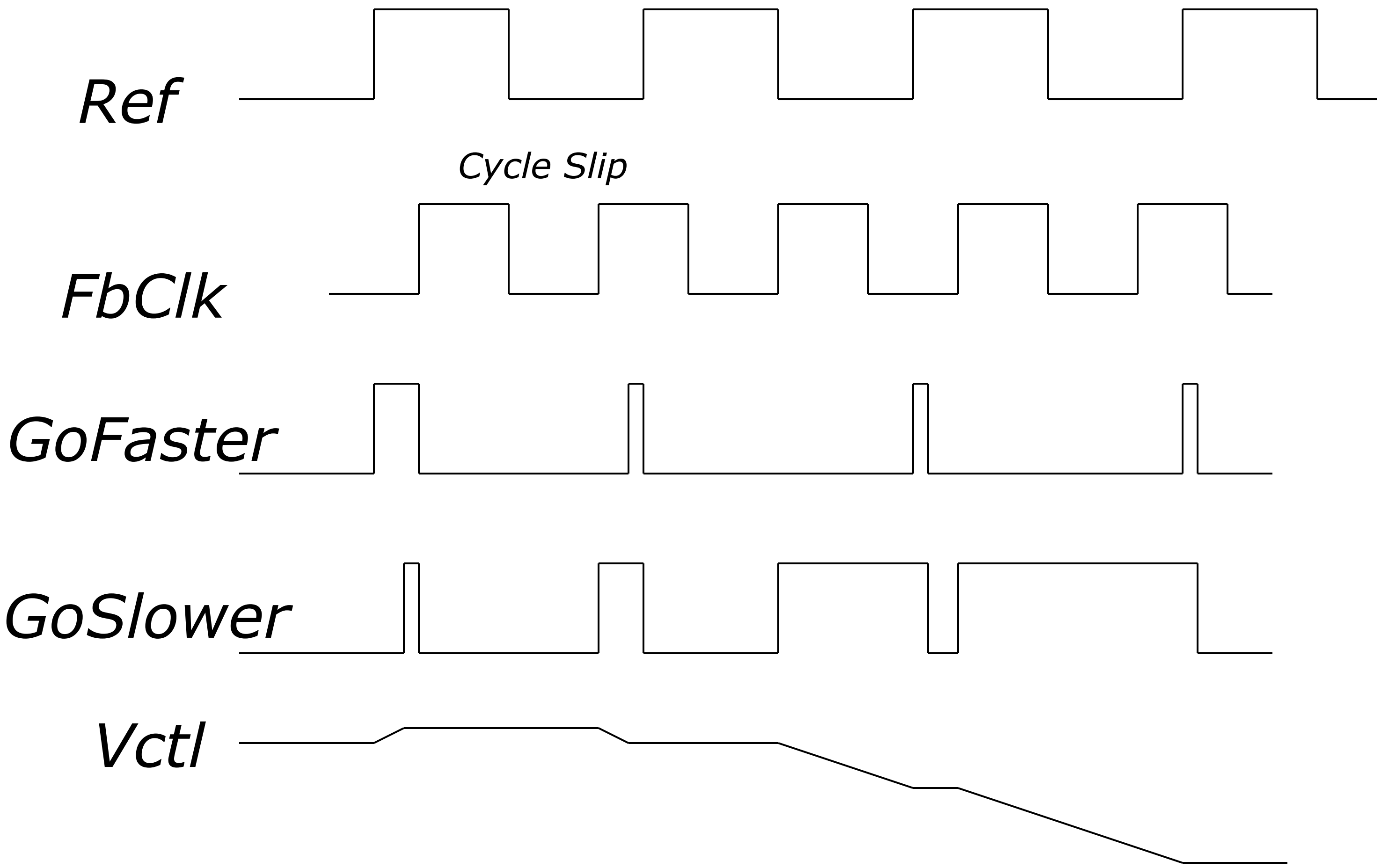
Phase-Frequency Detector(PFD)

PFD Block Diagram

- Edge-triggered - input duty-cycle doesn't matter - frequency correction takes precedence over phase correction – no harmonic locking – 3 state operation
- Output pulse-widths proportional to phase error
- Delay to remove "dead-zone"
- Symmetric NAND used to balance equalize delays from both inputs

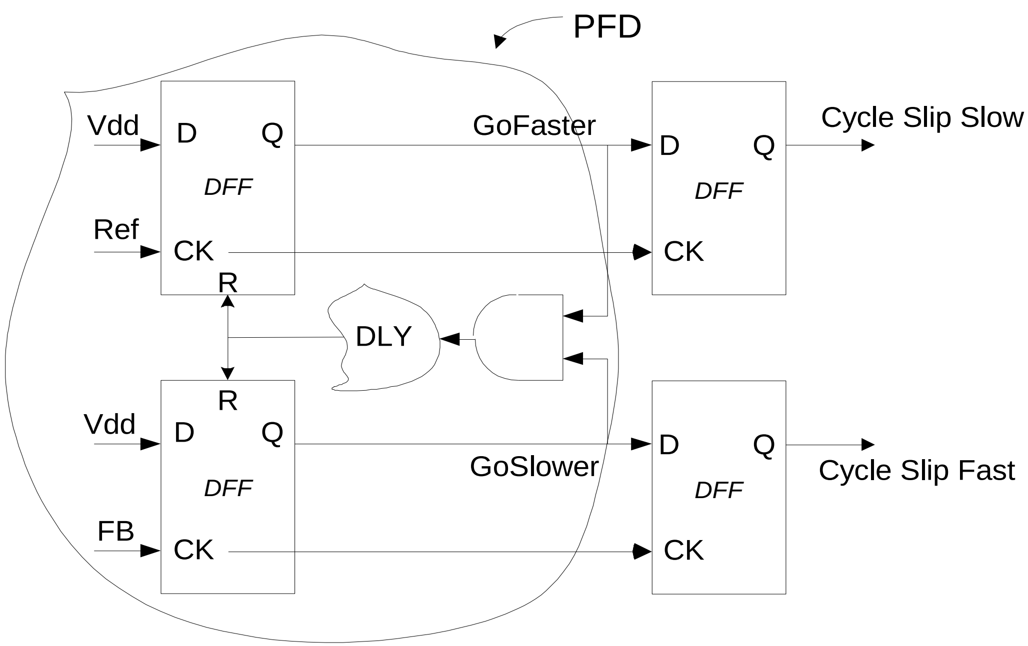


Example: PFD



Frequency Lock Detector

- Sample PFD GoFaster signal with rising REFCLK
- Sample PFD GoSlower signal with rising FBCLK
- If either sampled signal is TRUE, then PFD detected two consecutive REFCLK's or FBCLK's → cycle slip and loss of frequency lock
- May apply "sticky bit" to result to capture temporary loss of lock



Charge Pump(CP)

Charge-Pump Wish List

- Equal *UP/DOWN* currents over entire control voltage range - reduce static phase error
- Minimize mismatch caused by finite current sources g_{ds} and V_t mismatches
  - $\Delta V_t \sim 1 / \mathrm{sqrt}(W*L)$
  - long L in current sources for higher g_{ds}
  - Stacked (a.k.a common) gates in Isources help w/mismatch
  - use replica-bias CP and feedback amplifier to balance I_{up}/I_{down} – beware of mismatch between two CP cells
  - increase in CP's phase noise due to finite BW of this feedback?

- Minimal coupling to control voltage during switching and leakage when off - reduce jitter and phase drift
- Insensitive to power-supply noise and process variations – loop stability

Charge-Pump Wish List

- Minimize coupling caused by "clock feedthrough" (C_{gd}) and charge-injection
  - ½ sized dummy switches to reduce charge-injection
    - $Q_{inj} \sim ½ * C_{ox} * (W*L) * (V_{gs} - V_t)$
  - Small (and/or limited swing) switches to reduce clock feedthrough – watch for leakage with limited-swing
  - Balance timing and slew rates of all inputs

- Minimize PFD pulsewidth to minimize phase noise while still avoiding dead-zone (< 100 ps possible in 65nm)

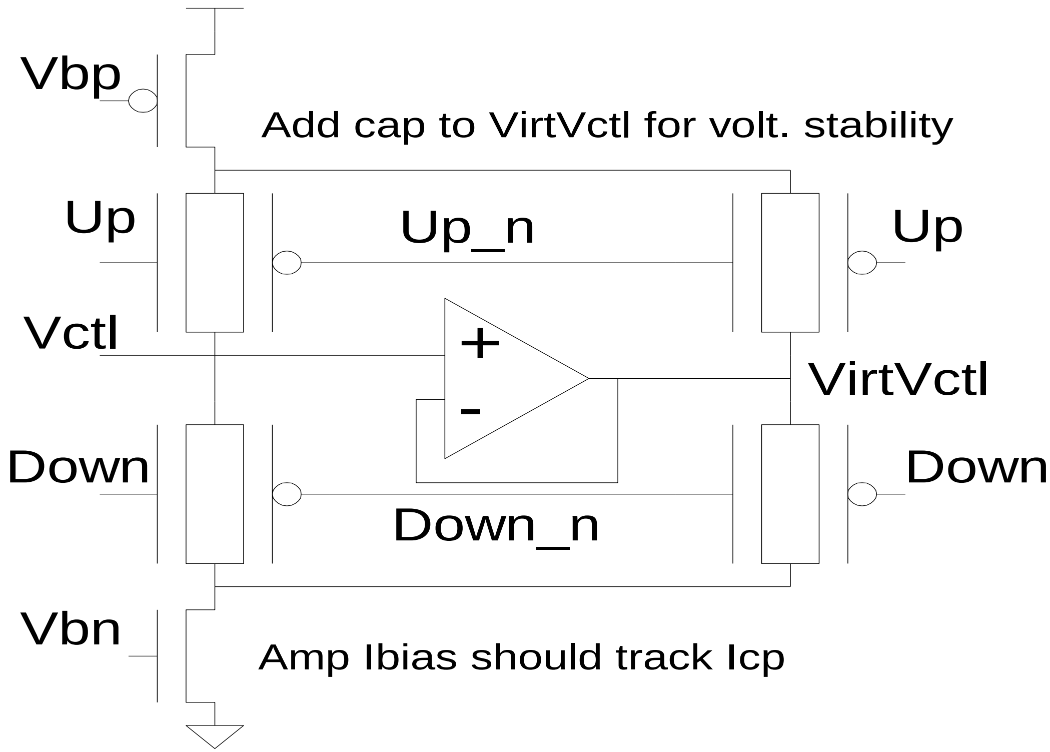
- Typical Icp: 5µA (mismatch)< I_{cp} < 50 µA (ΔV_{ctl})

Static Phase Error and CP Up/Down Mismatches

- Static Phase Error: in lock, net *UP* and *DOWN* currents must integrate to zero
  - If *UP* current is 2× larger, then *DOWN* current source must be on 2× as long to compensate
  - Feedback clock must lead reference for *DOWN* to be on longer
  - $T_{err} = T_{dn} - T_{up} = T_{reset} * (I_{up}/I_{dn} - 1)$
- Narrow reset pulse → generally lower static error
- Typical static phase error < 100ps
- Static phase error → period jitter @ T_{ref} (reference spurs)

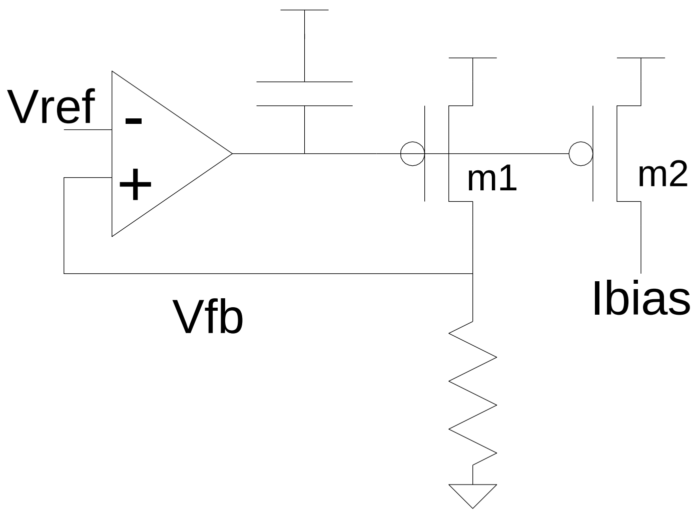
Charge Pump: const I with amp

- Amp keeps V_{ds} of current sources constant (Young '92), sinking "waste" current when UP, DOWN off
- Replica-bias ckt and additional amp used to set bias V_{bp}, setting $I_{up}=I_{dn}$. Start-up needed for V_{bp} bias *(not shown)*

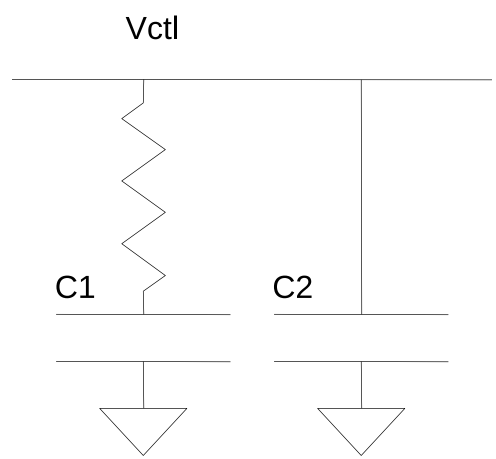


Bandgap-based I_{bias}

- $I_b \sim V_{ref} / R$
- V_{ref} generated from PVT-insensitive bandgap reference
- Con: feedback loop may oscillate
  - capacitor added to improve stability
  - resistor in series w/cap provides stabilizing zero *(not shown)*
- Pro: VDD-independent, mostly Temp independent
- Pro: Icp*Rlpf = constant → less PVT-sensitive loop dynamics



Low-Pass Loop Filter (LPF)



Loop Filter Basics

- Simplest and most commonly-used loop filter is continuous-time, passive filter
- Filters high-frequency phase error information from PFD/CP while integrating low-frequency error info onto C1 cap to set avg. freq - affects bandwidth
- Provides a means of isolating phase correction from frequency correction – $I_{cp}*R_{lpf}$ – affects stability
- Filters noise spurs caused by sampling – C_2 cap – adds parasitic pole at $1/RC_2$
- Other options include digital(FSM-based) filter, sampled-time filter (see Maneatis, Maxim) , and continuous-time active filter
- Differential designs can reduce sensitivity to VDD and substrate noise and often area by 2×. Requires common-mode feedback loop.

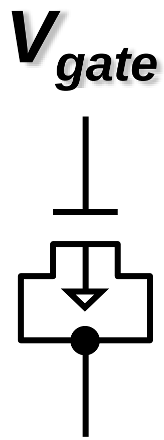
Passive, Continuous-Time Loop Filter

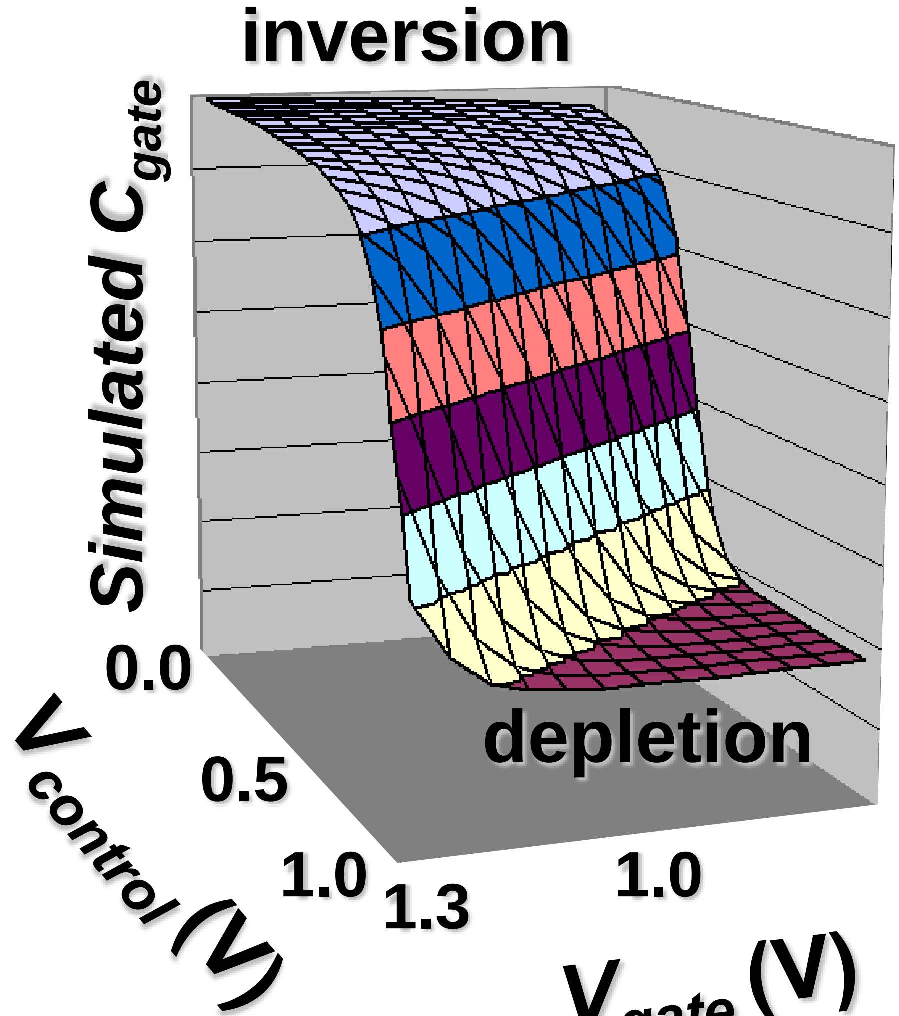
- R may be programmable
  - Avoid gate leakage and noise coupling from switches and parasitic resistance at extreme control voltages

- Leakage in MOSFET caps may be a HUGE problem
  - Exponential I vs. V: $I_{leak} \sim V_{gate}^{4}$ (approximate)
  - Weak temperature dependence
  - I_{leak} vs. t_{ox} → ~2-3× per Angström
  - Use metal caps (10× larger) or thick-gate oxide caps to minimize leakage
  - If MOSFET caps, *accumulation* mode preferred – flatter C_{gate} vs. V

- Typical values:
  - $0.5k\Omega < R_{lpf} < 20k\Omega$
  - $5pF < C_1 < 200$ pF
  - 2% (low phase error) < C_2/C_1 < 10% (low period jitter)
  - Smaller caps are becoming more common w/ higher reference frequencies and metal cap usage

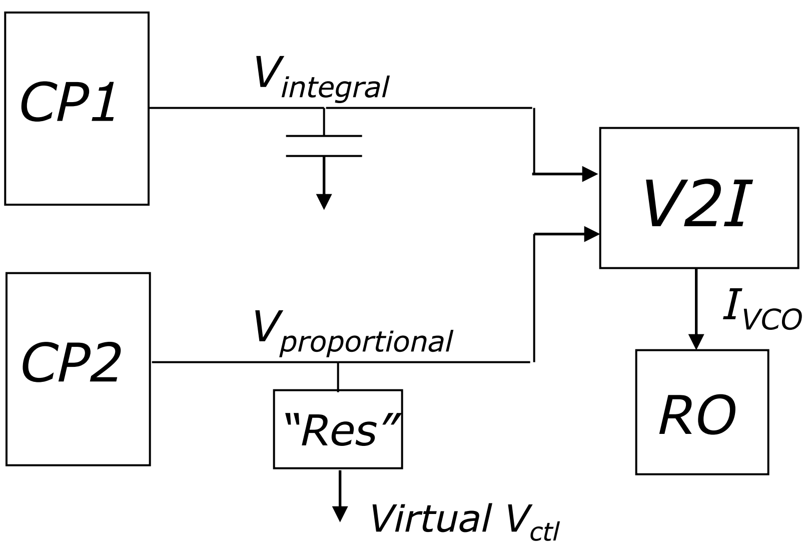
Depletion-Mode MOSFET C_{gate} vs. V





Feed-Forward Zero: eliminate R

- Resistor in classic LPF provides an instantaneous IR on the control voltage causing the VCO V2I to generate a current bump on the oscillator input
- Alternative: eliminate R → Add parallel CP path into V2I.
  - requires parasitic cap (C_2 *not shown*) to the proportional loop to reduce reference spurs
  - see Maneatis '96 for continuous time or '03 for sampled loop filter
- Reduces LPF phase noise? Commonly used in low phase-noise I/O apps.

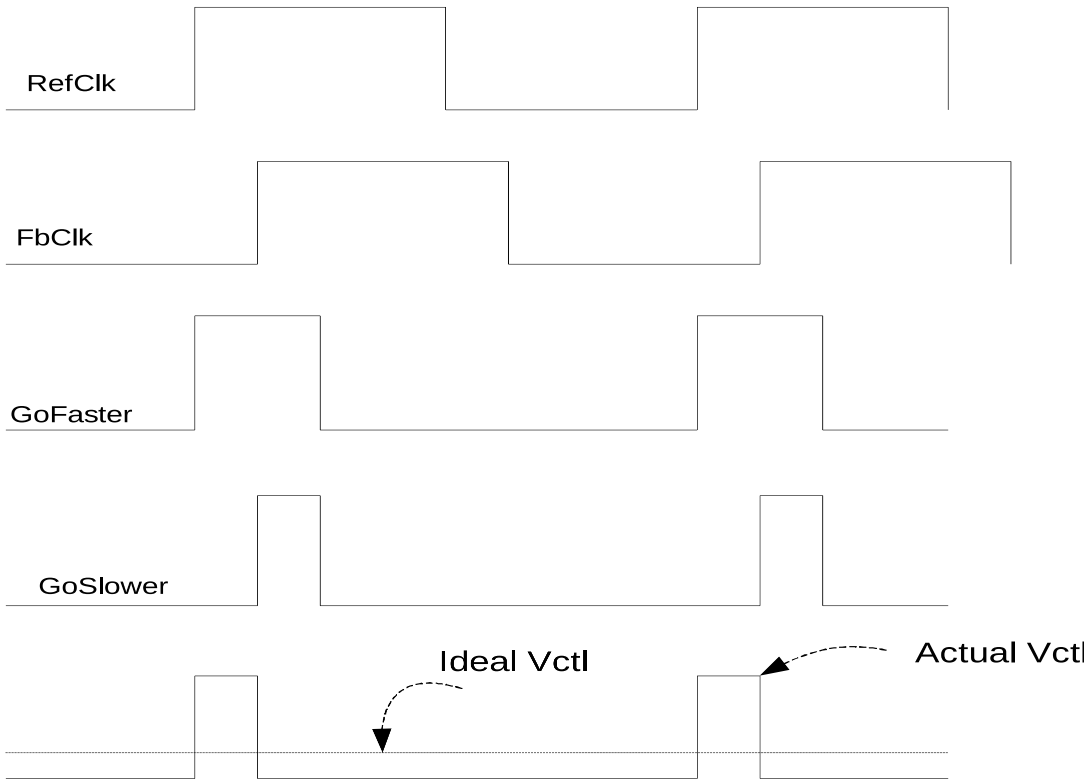


Dual-Loop Charge-Pump Mismatch

- Iup/Idown ratios in proportional and integral charge-pumps are partly uncorrelated due to random device mismatch
- Net charge from integral CP must integrate to zero for stable frequency – determines static phase error alone
- Net charge from proportional CP causes frequency kick every PFD cycle (Kv*I*R) caused by static error and its own Iup/Idown mismatch
- Upshot: control voltage adjusts up or down from ideal level to achieve correct average frequency but f_{VCO} varies within PFD cycle (phase wander)– need well-matched CP's to avoid this effect

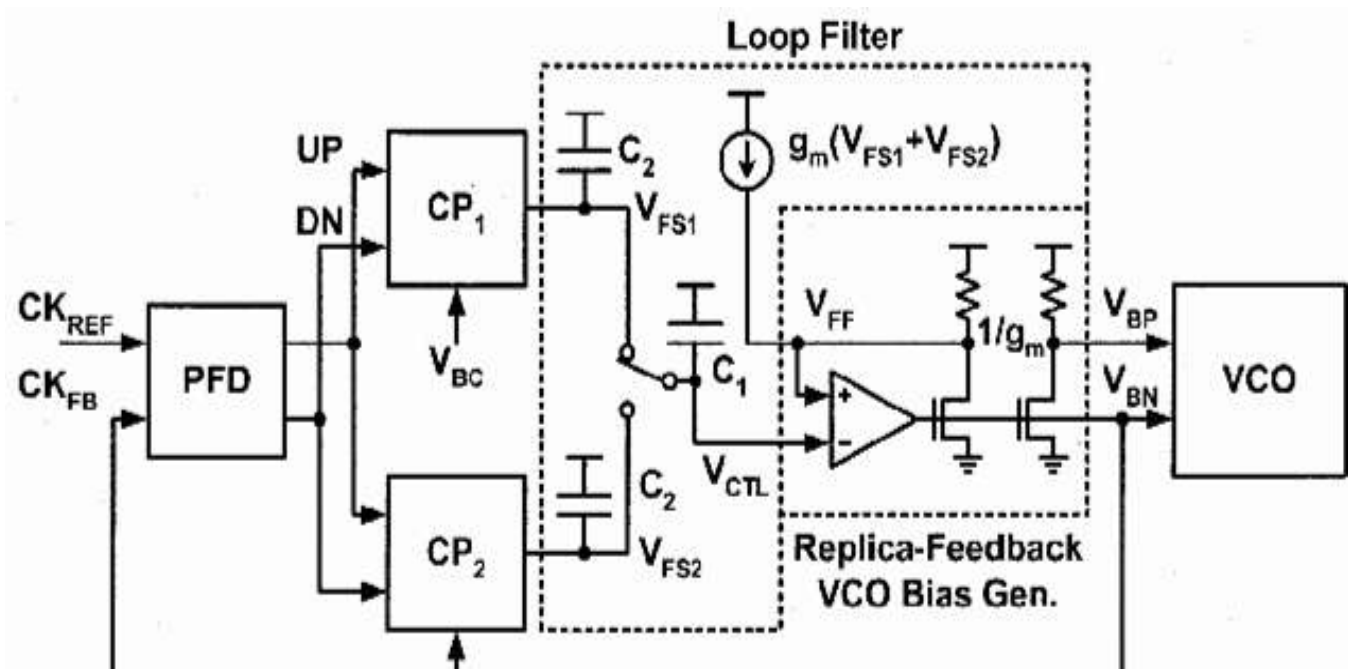
Dual-Loop Charge-Pump Mismatch

- Static error in integral charge-pump →period jitter and phase wander



Sample-Reset Loop Filters

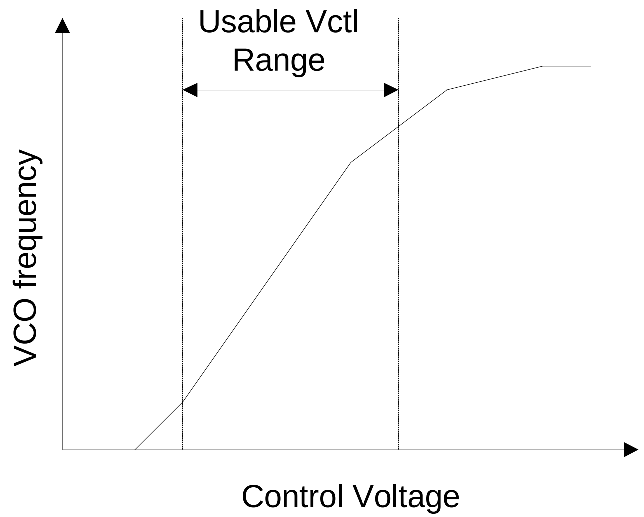
- Single charge-pump for I_{int} and I_{prop} – Zero ~ sqrt(C1/C2)
  - e.g. Maneatis (JSSC '03)
- Two charge-pumps to allow for reset (discharge) delay
- Spreads phase correction over Tref – can reduce ref spurs
- Mismatch between CP's → significant VCO phase modulation at $f_{ref}/2$



Voltage-Controlled Oscillator (VCO)

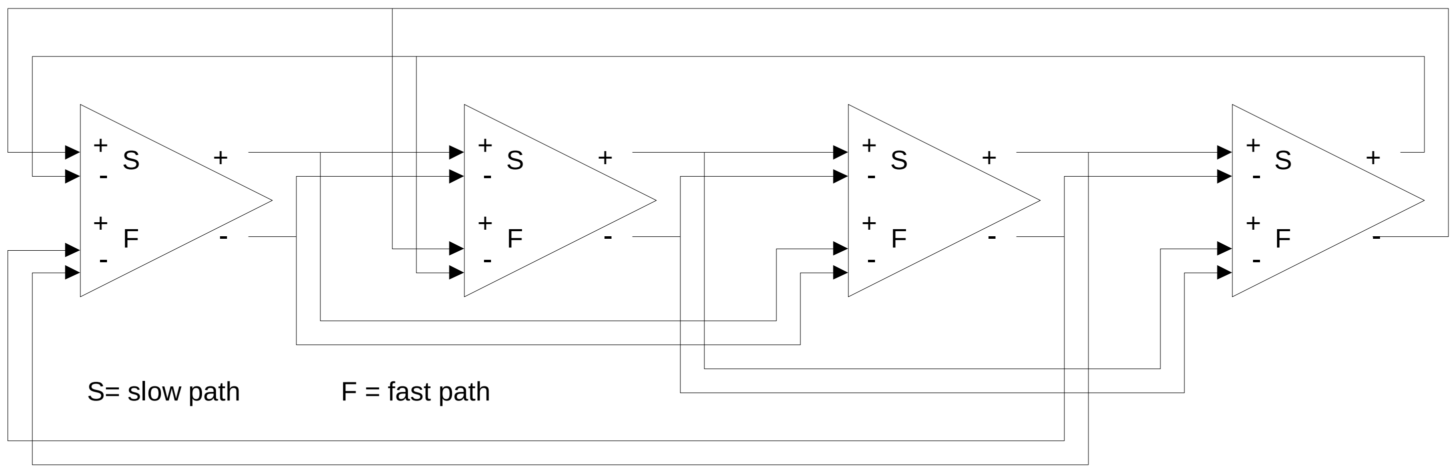
Voltage-Controlled Oscillator

- VCO usually consists of two parts
  - bias generator (e.g. V_{ctl} to I_{ctl})
  - voltage or current controlled ring oscillator (RO)
- Typical VCO gain: K_{vco} ~ 1-5× * f_{max}. May vary w/PVT by > 2×
  - need frequency range: >2× to allow for PVT
  - desire constant gain over most of usable control voltage range



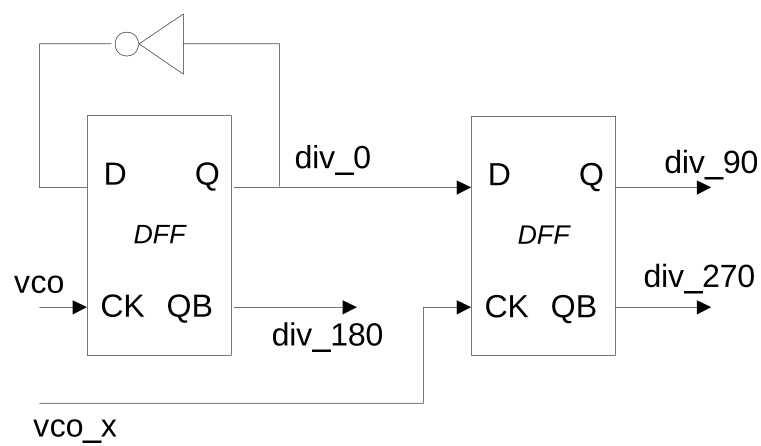
VCO w/Feed-Forward Path

- RO delay stage may receive inputs from multiple prior stages (e.g. N-1 and N-2)
  - allows N-stage VCO to oscillate at speeds otherwise attainable only by reducing # of stages
  - easier to implement with differential signals
  - extra care must be taken to ensure that RO will safely oscillate



Voltage-Controlled Oscillator

- Barkhausen criteria for sustained oscillation
  - loop gain must exceed 1, loop phase must equal 360°
  - more delay stages → easier to initiate oscillation
  - gain(DC) > 2 for 3 stages, gain > sqrt(2) for 4 stages
- Quadrature clocks (0°, 90°, 180°, 270°)
  - requires 4 delay stages or
  - divide "differential" VCO outputs by 2, then delay one set of divided outputs by ½ T_{vco} to generate quadratures. Allows any # of delay stages



PLL Suppression of VCO Noise

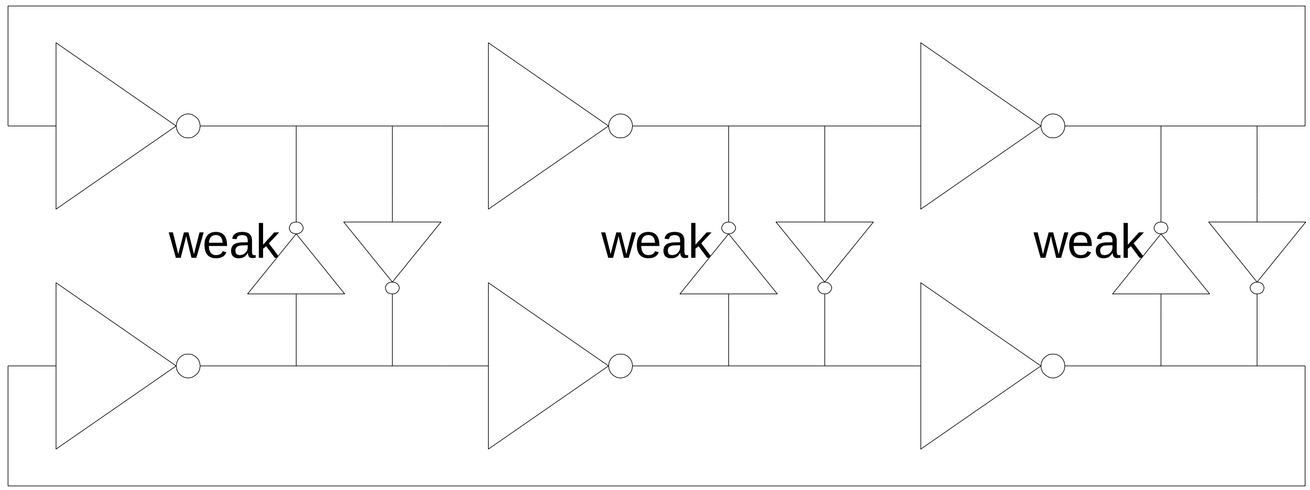
- PLL acts like a high-pass filter in allowing VCO noise to reach output
- Need noise-immune VCO to minimize jitter
  - Feedback loop cannot react quickly.
  - Tradeoff between tuning range & noise sensitivity
- Power-supply noise is usually largest source of VCO noise
- VCO power-supply sensitivity should be at least 10-20$\times$ less than inverter

PLL Suppression of VCO Noise

- High power, fast edges, large swing → low random jitter
  - J_{rms} ~sqrt(kT/2NC) / (f_{vco}*V_{swing})
    - where N=#of stages, C=cap/stage
- Match rise/fall times, inter-stage delays to minimize phase noise (lowers ISF)
- RMS random jitter (*kT*) < 0.2% VCO period (typical)

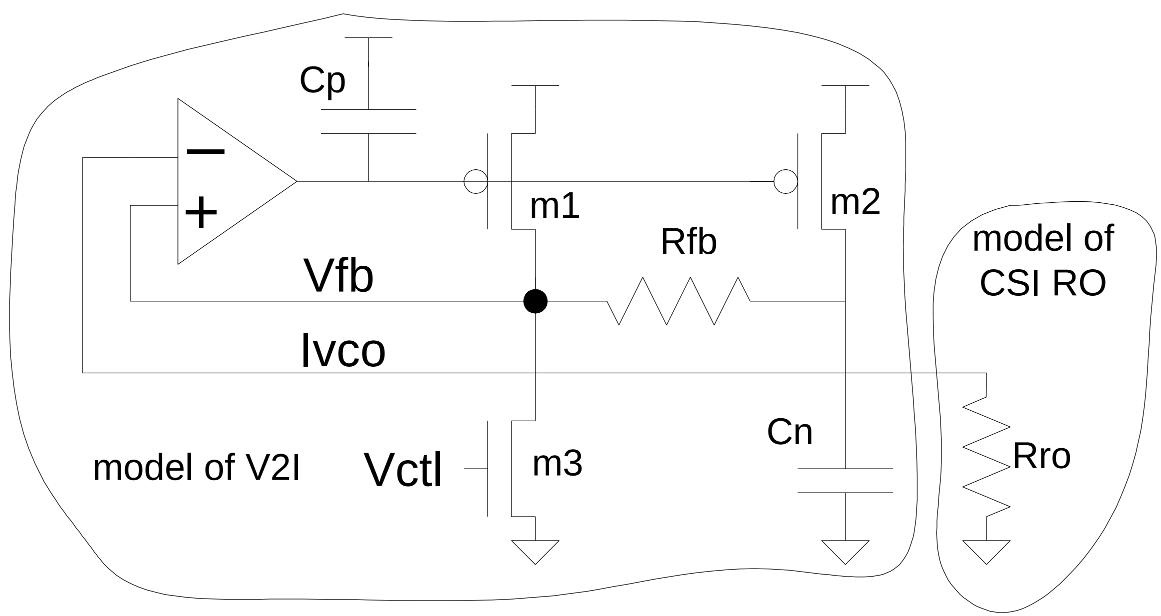
VCO w/current-starved inverters(CSI)

- Usually odd # of stages (usually 5+)
- Feedback INV → usually weaker by ~4×
- Tune frequency by adjusting "VDD" of inverters – changes delay
- "Vdd" for inverters is regulated output of VCO V2I



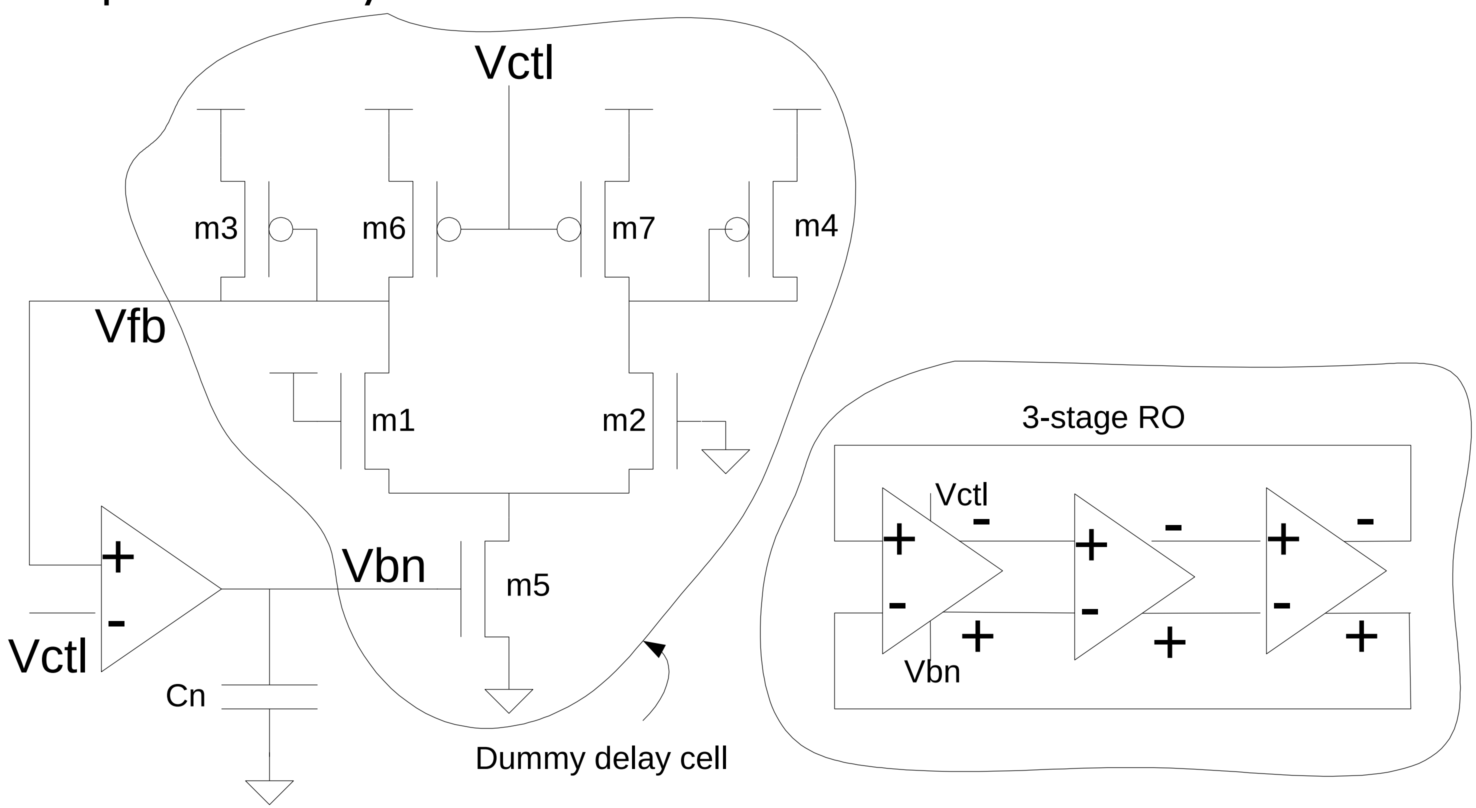
V2I for CSI (V. von Kaenel (JSCC ’96)

- Bias circuit for current-starved inverter-based ring oscillator
- Feedback → amp provides good low-freq power-supply rejection
- Caps to Vdd and Vss provide good high-freq rejection but add parasitic poles → e.g., $\varpi_p = 1/(R_{ro}*C_n)$
- Start-up necessary. Stability a concern



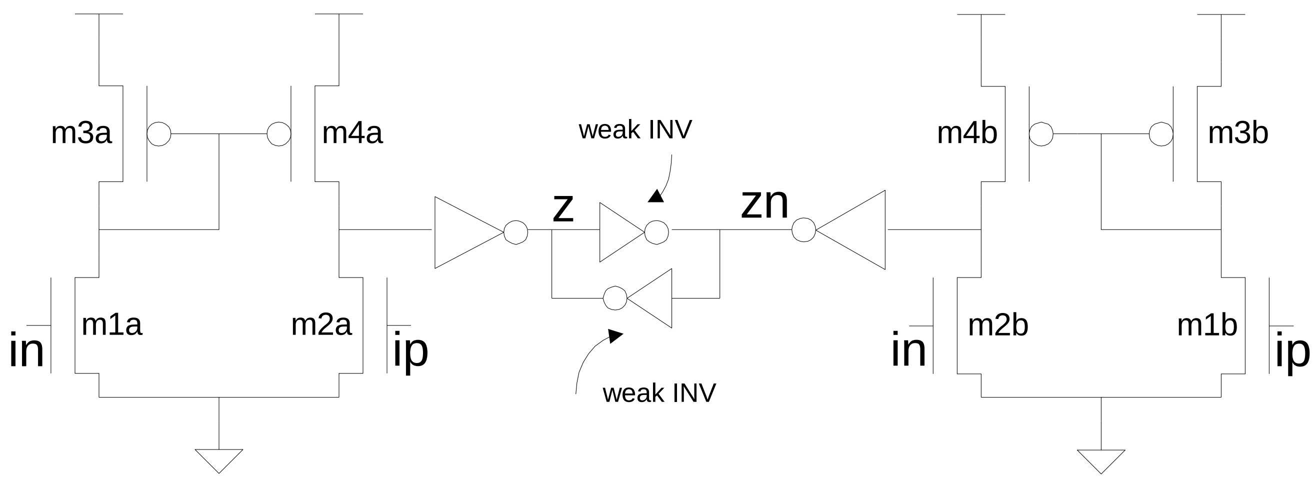
Diff-Amp VCO w/Replica-Bias V2I

- $V_{swing} = V_{ctl}$ (Maneatis '96)
- Amp provides DC power-supply rejection
- Stable, but getting high BW and good PSRR tricky
- Start-up necessary



VCO: Level-Shifter

- Differential-pair without tail current
- Need sufficient gain at low VCO frequency – use low-V_t NMOS
- Use NMOS input pair if VCO swing referenced to VSS for better power-supply rejection
- For best duty-cycle, use two instances of level-shifter (swap inputs), and couple complementary outputs with weak inverters
- Typical duty cycle: 50 ± 3% with random mismatch



Feedback Divider

Feedback Divider (FBDIV)

- Typical Implementation: synchronous digital counter
- Max FBDIV frequency should be greater than max VCO frequency to avoid "run-away"
  - beware of Synthesized, Placed & Routed designs
- Counter output may glitch → re-sample with VCO output to clean up glitch, reduce latency and phase noise
- Loop Phase Margin Degradation ~ $\varpi_{c*}T_{fbdly}$
  - usually insignificant (a few degrees)
- Divider may be internal to PLL or after clock tree to cancel clock tree skew
- May provide additional output signals used to deterministically synchronize tester controls to VCO clock and/or walk signals between various on-chip clock domains

Auxiliary Circuits

Voltage Regulator

- Provides stable, PVT-insensitive, clean power-supply for PLL
  - lower jitter, phase noise
  - more stable loop dynamics, VCO range, etc.
  - aim for > 30dB PSRR, definitely > 20dB
- Uses bandgap reference to set voltage and bias current levels
- Two voltage regulators sometime used
  - High VDD for charge-pump (analog) and lower VDD for VCO
  - “Quiet” for analog (CP, VCO bias) and “Dirty” for digital (PFD, FBDIV)

Voltage Regulator

- Requires higher power-supply (e.g., 1.8V → 1.2V)
- Wastes current
  - higher VDDA and bandgap/regulator over-head (0.5-3mA).
  - aim for current overhead < 20%. <5% is achievable in some apps
- Regulator area (inc. bandgap) is small compared to decoupling cap area
  - Area (MOSFETs, Rpoly, diodes) ~ 70 x 70 μm^2 (65nm)
  - Area (DECAPs) ~ 125µm x 125um for 100pF (65nm)
  - Typical cap ~ 30-200pF
- V_t-mismatch in bandgap amplifier input pair dominates overall regulator mismatch
  - 3mV offset at amp →~20mV variation at output
  - Goal < 25mV 1-σ variation from device mismatch
  - Goal < ±5mV PVT variation (due mostly to diodes)

Digital PLL’s

Why a Digital PLL?

- Replaces process and noise-sensitive analog circuits with digital equivalents – advances on work with digital DLL's
- Increases PLL design portability and testability
- Takes advantage of area scaling with nm devices
- Greater flexibility in loop bandwidth – don't need huge capacitors for low BW
- Increases ability to test and observe. e.g. open-loop, disturb loop
- Fast behavioral simulation
- "Good-enough" for frequency synthesis applications
- ISSCC presentations: TI('04) and IBM ('07)

Why NOT a Digital PLL?

- Usually not “good enough” for phase-tracking applications
- VCO frequency has finite frequency resolution (e.g. 10-14 bits). May use coarse DAC if high-frequency dithering available
- VCO has limited range – requires range control and/or calibration
- VCO may have poor noise rejection if purely digital frequency control and no voltage regulator (usually analog)

Why NOT a Digital PLL?

- Need high-frequency over-sampling clock for sigma-delta loop filter – VCO? Refclk? Start-up problem?

- TimeError-to-Digital Converter is hard – poor resolution, high power – usually < 5 bits – is Bang-bang an alternative? FbDiv internal state contains phase error information

- Digital filter generates large noise spurs, possibly inducing jitter, and dissipates more power than passive loop filter

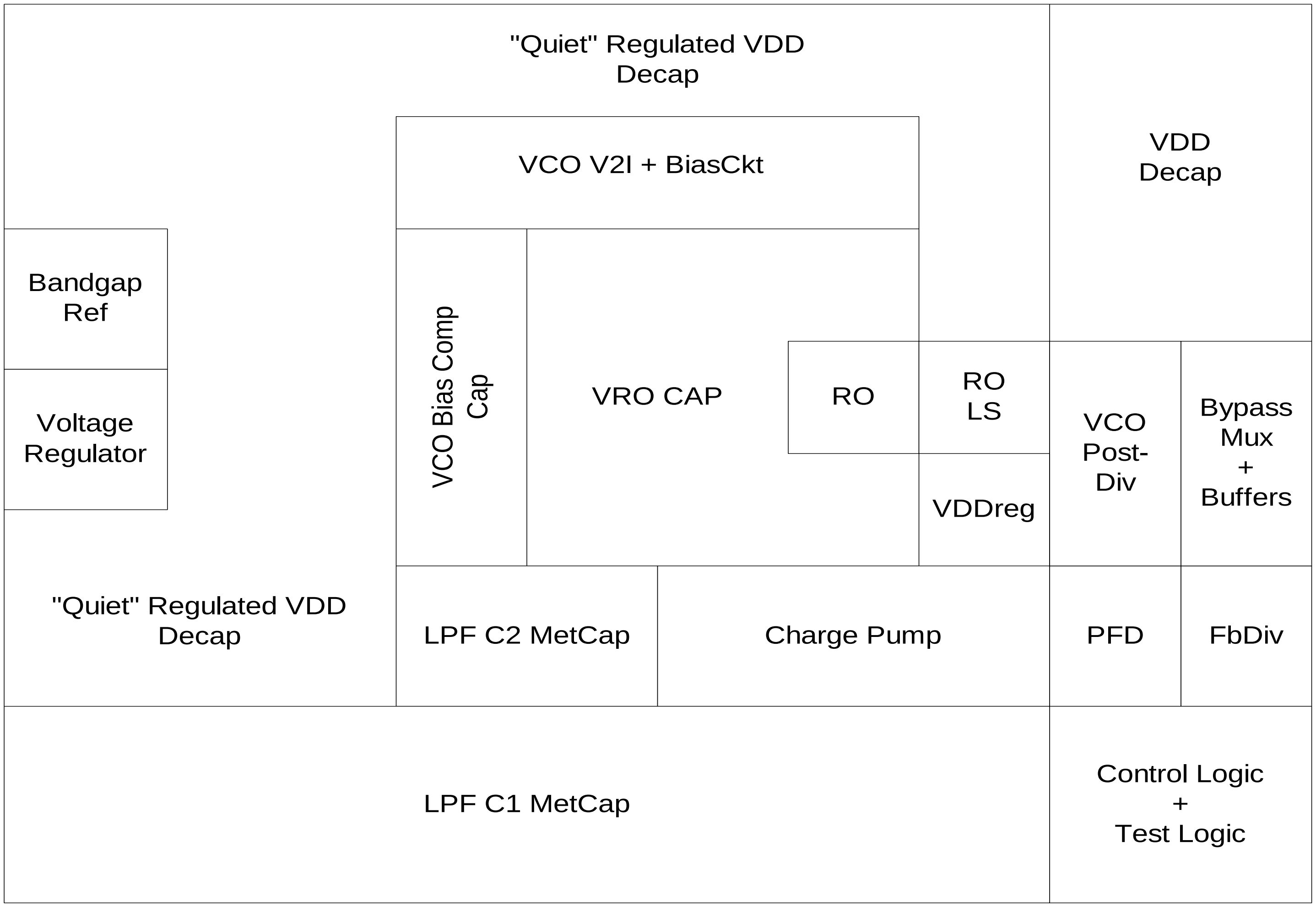
- Generating proportional correction can be tricky

What is a Digital PLL?

- Replace charge-pump (time error-to-charge) with TimeError-to-Digital Converter
- Replace loop filter with discrete-time digital filter (usually 2nd or 3rd order sigma-delta)
- Replace voltage-controlled VCO with digital-control (vary cap load, interpolation, etc.)
- Are analog components “allowed”? Voltage regulator? Analog current-steering DAC for VCO?
- Sampled-system modeled in the Z-domain

Circuit Verification

PLL Floorplan



Noise Isolation

- Check extracted netlist for coupling of switching signals onto sensitive analog signals (e.g. REFCLK → V_{ctl})
- Check that LPF metal caps are present and well-connected to correct power supplies
- Check that VSS of LPF metal caps and VSS of VCO bias circuits are well-connected and at same potential
- Check that correct shields for sensitive signals are in place and well-tied to correct power supplies

Noise Isolation

- Account for parasitic capacitance to substrate in “NWELL” decaps, diodes, and well/diffusion resistors
- Add guard rings as applicable
- Buffer control signals and programmable inputs locally before use
  - avoids problem where GND of control signal doesn’t match local GND where signal is used
  - filters coupling/glitches on long routes

Signal EM / ESD

- Inspect wires that conduct DC current and wires that drive large switching output loads for EM violations (e.g. charge-pump bias, output clocks)

- Check that signal ESD and/or power supply clamps are well-connected to power supplies (< 1-2 Ω)
  - extract power grids and ESD
  - simulate for voltage peaks and diodes wired-backward

Power-Grid IR

- Aim for avg IR drops < 5mV over entire PLL, less within and between related analog blocks
- Decoupling capacitors surround large, switching buffers to reduce IR drops and are well-connected to grid
- Check for isolated power domain islands
- Plan power domains and level-shifter placement up-front

Switching Signals

- Match differential signals – total capacitance and coupling (e.g. up, up_x, dn, dn_x, clk, clk_x)
  - try to match total capacitance < 1-2%

- Maintain fanout (incl. Wires) < ~6 on high-speed paths, < ~10 on DC paths (e.g. encode/decoders)
  - reduces crow-bar current and noise glitches

- Setup/Hold checks in PFD, Feedback Divider, and Post-VCO divider. Needs lots of margin for FBDIV to account for overshoot, aging, etc.
  - strive for FBDIV faster than VCO(max)

PLL Instantiation – Visual Checks

- Mismatch on differential signals
- Coupling into refclk, output clocks
- Possible glitches on control inputs
- Signal routes over sensitive areas of PLL (VCO, loop filter, charge-pump)
- Large buffers on edge of PLL that may inject noise in substrate (keep-out requirement?)

PLL Instantiation – Visual Checks

- Output wires wide enough to handle current load (EM)
- Rise/fall times on inputs/outputs – add max_cap limit into timing file to flag heavy loads
- VDDA/test signal routes to bumps and/or ESD
- VDD/ VSS power supply connections

Functional Modes

- Power-Down/Reset/Test Modes
  - chicken-and-egg start-up problems – esp. level-shifters, boot-strapped regulators
  - Contention?
    - measure current in every device in these modes
- SLOW clock mode
  - drive slow clock at power-on to remove contentious states in downstream logic
  - disable any clock gaters
  - mux in separate ring oscillator or force VCO/post-VCO div to produce low frequency clock in open-loop mode
  - avoid glitches when entering/leaving SLOW mode
- Frequency Hopping
  - Ensure that FBDIV can't fail during frequency transition if RESET not applied

Power/Clocking Domains

- Level-shifters are present when crossing power domains and are connected to correct supplies
  - apply writability analysis with mismatch
  - check for overstress
  - easy to miss
- Add synchonizers or “walk clocks” when crossing clock domains – easy to miss
- Check metastability on flops, comparators – is there a failure mechanism? Calculate MTBF.
- Insert bypass mode mux, preferably such that if the regulator fails, bypass clock still propagates to output

RTL vs. Circuit

- Add assertions to RTL model to flag illegal input states
- Verify that RTL and tester don’t assume that dividers, etc. are initialized to known states upon power-on, frequency-changes, etc. – add logic to establish determinism if needed
- Model/verify all digital logic in RTL
- Specify expected input states at all analog blocks in various operating modes
- Simulate PLL exhaustively in VerilogA, Nanosim, etc, if possible

RTL vs. Circuit

- Look for incorrect polarity on input control signals (e.g., reset, powerDown) and REFCLK
- Look for glitches on feedback clock and other dividers
- Exercise all divider/counter states
- Check for possible VCO run-away conditions during power-on and frequency changes (e.g., no reset or feedback divider is halted)
- Verify that unselected inputs of muxes in critical signal paths are gated (e.g., VCO post-divider muxes)

Behavioral Simulations

- Behavioral simulation –before detailed circuit design define requirements for each block – e.g. PLLUS, Simulink
- Develop/verify jitter budget – e.g. PCI-Express
- Estimate VCO frequency overshoot
- Loop bandwidth vs. reference noise suppression
- Simulate effects of loop filter leakage, charge-pump mismatch, feedback delays, OSR, spread-spectrum tracking, Vctl-sensitive loop parameters, PFD dead-zone, parasitic poles

Circuit Simulations

- Start-up circuit safety margin - bandgap, VCO, regulators
- Stability of all internal feedback loops
  - AC and transient impulse response
  - e.g., bandgap, regulator, charge-pump bias, VCO bias
  - Phase margin, gain margin, # of rings
- VCO - RO stage delays rise vs. fall, stage-to-stage – lower ISF
- Level-shifters' possible corruption of duty-cycle
- Switching-induced noise spikes on regulated power supplies
- Current dissipation in power

Circuit Simulations

- PSRR of voltage regulators, ability of regulators to meet fast-changing current load
- Step reference phase, observe PLL re-lock
  - overshoot, relock time
- Simulate entire sequence from power-on to lock
  - sanity check

Devices/Circuits

- Estimate effects of Vt mismatch BEFORE starting layout (monte carlo, dVt ~ 1/sqrt(W*L))
  - most sensitive: bandgap, charge-pump, other low I ckts
- Estimate loop parameter variations, static error, reference spurs due to PVT and mismatch before starting layout
  - Kv, Icp, R, C1 (also vs. Vctl) – esp. dual- charge-pump designs
  - circuit techniques to minimize effects: self-bias, Icp*Rlpf=const
  - self-bias not as effective if not all devices the same Leff
- Diode current density (bandgap) – ideality factor may be sensitive to current density – stay away from cliff

Device Reliability

- Gate Overstress
  - especially likely during power-down, reset, test
  - hspice .biaschk is useful

- Gate Leakage
  - LPF especially, I_{leak}(LPF) < a few nA
  - Switches used for test modes
  - Gate loads of high-impedance nodes (e.g. bandgap)
  - Large op-amp inputs

Device Reliability

- Verify that circuits with PMOS devices are not NBTI-sensitive
  - V_{gs} of matched devices should be the same at all times, even when not selected (e.g. current-steering DAC) – don't place switches closest supply rails
  - switching circuits such as VCO and FBDIV should have enough frequency headroom to allow for aging. High V_{gs} is bad! 10-20% margin?
  - effect worse at 45nm and 65nm and may not be well-modeled

Lithography/Devices

- Add dummy poly to reduce ACLV (across chip linewidth variation), esp. in L_{min} devices

- Maintain gate poly on fixed pitch in same orientation to reduce ACLV (esp. in L_{min} devices)

- Try to maintain constant poly density – e.g. no large caps next to sensitive L_{min} devices)

- Add dummy devices if stress/strain is applied and matching is required (e.g., charge-pump)

Tips for Design for Test

- Measuring Jitter and Phase Error
- Measuring Loop Dynamics
- Analog Measurements
- Probing

Getting Clocks from PLL to Board

- Differential I/O outputs highly desirable to reject common-mode noise – use fastest I/O available

- Divide VCO to reduce board attenuation only if necessary → make divider programmable

- Measuring duty-cycle
  - Divide-by-odd-integer
  - Mux to select either true or inverted VCO clock. Duty-cycle error = (Duty+ - Duty-) / 2

Getting Clocks from PLL to Board

- Ability to disable neighboring I/O when measuring jitter

- Observe REF, VCO, and FBCLK. Gate unused inputs to the clock source mux

- Phase error measurement: trigger scope on REFCLK on board. Capture internal REFCLK and FBCLK in infinite persistence. Measure difference between internal REFCLK and FBCLK on *same* pin.

Measuring Loop Dynamics

- Modulate reference phase at various modulation frequencies and measure VCO phase using TIE
  - used to construct closed-loop transfer function

- On-chip state-machines
  - range from simple to sophisticated
  - disturb locked PLL in some way and observe re-lock behavior

Analog Measurements

- Need ability to measure key internal analog signals without injecting noise
  - Loop filter control voltage
  - Ring Oscillator regulated supply
  - Bandgap reference
  - Regulated power supplies
  - Charge-pump bias voltages and currents
- Metrics
  - Measurement BW ~ PLL Bandwidth or less
  - Accuracy ~ 5mV?
  - Programmable via JTAG

Analog Measurements

- Internal A/D
  - Can be fairly slow
  - Minimize mux switch leakage into A/D front-end
  - Minimize coupling to sensitive signals
  - May require external analog pin for calibration
  - Compare analog voltage to internally-generated voltage reference
  - Use state-machine to minimize # of comparators to save area
  - Disable when not in use to save power

Analog Measurements

- Analog Observation Pins
- Pass-gate mux connects analog signals to outside world
- Force or sense voltage/current
- Low BW – high impedance analog signals and high parasitics
- Need ESD (HBM,CDM) to protect signals –watch for leakage
- Buffer control voltage before sending off-chip to prevent leakage and extra load from upsetting feedback loop – watch for gate leakage in unity-gain buffer
- Pull-down to VSS far-side of pass-gates when not in use to minimize coupling of noisy pin to analog signals (at expense of increased leakage). Disable pull-downs for ESD testing
- Can wire-OR analog observation pins from several PLL's but watch for increased pin leakage causing IR drops across pass-gates (e.g., 3-6kΩ) or causing high-impedance analog signals to droop

Probing On-chip (last resort!)

- If not flip-chip, then put probe pads on top-layer metal
- Probe pad size >1μm × 1μm. Prefer > 2μm × 2μm
- Place probe pad on a side-branch of analog net to avoid breaking wire with probe
- Separate probe pads to allow room for multiple probes
- FIB: can add probe pad, add or remove wires
  - need room and luck

Summary: Uncle D’s PLL Top 5 List

1. Maintain damping factor ~ 1 for low period jitter apps

2. VDD-induced and intrinsic VCO noise – loop can’t do the work for you

3. Leaky loop filter gate caps will cost you your job

4. Make FBDIV run faster than VCO

5. Observe VCO, FBCLK, REF, clkTree on differential I/O pins – you can’t fix what you can’t see!

Special thanks to Alvin Loke for allowing to me “borrow” some of his diagrams and ideas for this talk…which ones? The good ones

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PLL Failures

PLL Failures

- Observation is that VCO frequency is pinned at max value. Can’t observe Vctl or feedback clock. VCO fails to oscillate at low frequency because of insufficient gain in 3-stage VCO. When VCO finally starts, FBDIV can’t keep up, causing “run-away” Solution: increase gain of delay stage and FBDIV speed.
- VCO “run-away” when re-locking to higher frequency due to VCO overshoot and slow FBDIV.
- VCO loses lock occasionally at low frequencies. Due to insufficient VCO level-shifter gain. Dropped VCO edges. Required real-time scope for debug
- High jitter at low VCO frequencies due to Vctl approaching Vt of V2I current source. Solution: operate VCO at 2X.

PLL Failures

- Occasional high deterministic jitter caused by coupling into PLL's VDDA bondwire.
- Extremely high period jitter – caused by incorrect wiring of 8-bit charge-pump setting. Bandwidth much too high. Verilog model did not check for legal input settings.
- PLL won't start-up at low temp due to weak start-up circuit in voltage regulator and lack of simulation at corners with slow VDDA ramp-rate.
- PLL period modulated strongly by 400MHz signal, resulting from oscillating internal feedback loop in VCO bias ckts. Ultimate cause, fab misprocessing of compensation cap and insufficient margin in ckt.

PLL Failures

- Metastability condition corrupted digital loop filter due to slow devices, low Vdd, and insufficient design margin.
- Digital VCO out-of-range due to resistor mis-processing. Solution: fusable chicken-bits to adjust frequency range.
- Race condition in digital loop filter caused by missing synchonizers in clock domain crossing.

PLL Failures

- CDM ESD failures of analog measurement pins – no visual inspection and no extraction/simulation of connection to VSS.
- Duty-cycle corruption (> 57%) – caused by unbalanced fanouts in delay stages after VCO – exacerbated by single-ended clocking.
- Contention in analog observation signals due to ESD diodes wired backward and control logic bugs.
- Inconsistent duty cycle. Failure to initialize state in post-VCO divider exposed VCO duty-cycle error.