An On-Chip All-Digital Measurement Circuit to Characterize Phase-Locked Loop Response in 45-nm SOI

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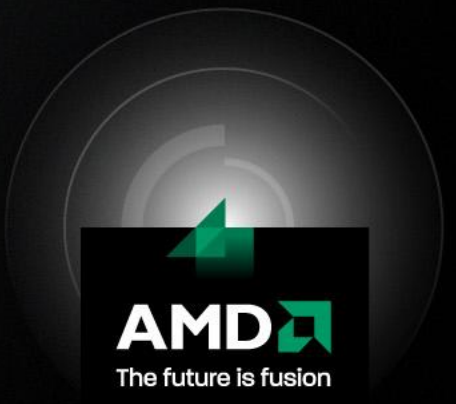


Outline

- Motivation
- Loop Measurement Circuit
  - Algorithm
  - Architecture
- Silicon Results
- Conclusion

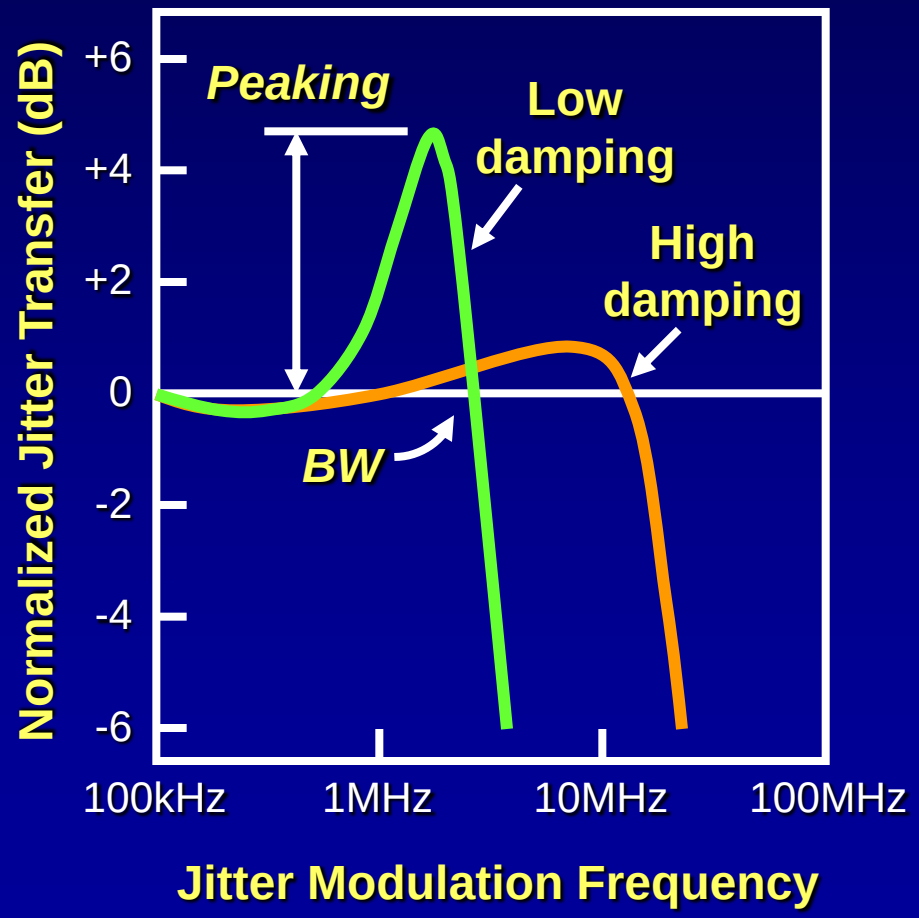
PLL Closed-Loop Transfer Function

- Frequency domain model
  - Input: "excess" phase *modulation* of input (reference) clock
  - Output: "excess" phase *modulation* of feedback clock

$$\phi_{refclk}(t) = 2\pi f_c t + \phi_{mod}(t)$$

PLL

$$\phi_{feedback}(t) = 2\pi f_c t + f(\phi_{mod}(t))$$



Motivation

- Strict bandwidth and peaking requirements
  - e.g., PCI Express Generation II @ 5 Gb/s
    - 5–8 MHz *BW* / < 1 dB peaking
    - 8–16 MHz *BW* / < 3 dB peaking
- Locktime (function of *BW*) increasingly important given frequent exit from sleep/power-save states
- Device PVT variation → simulations inadequate
- Standard methods
  - Spectrum Analyzer, Waveform Generator
- Problems with standard methods
  - Slow → expensive
  - Wafer? Package? Product? → inflexible

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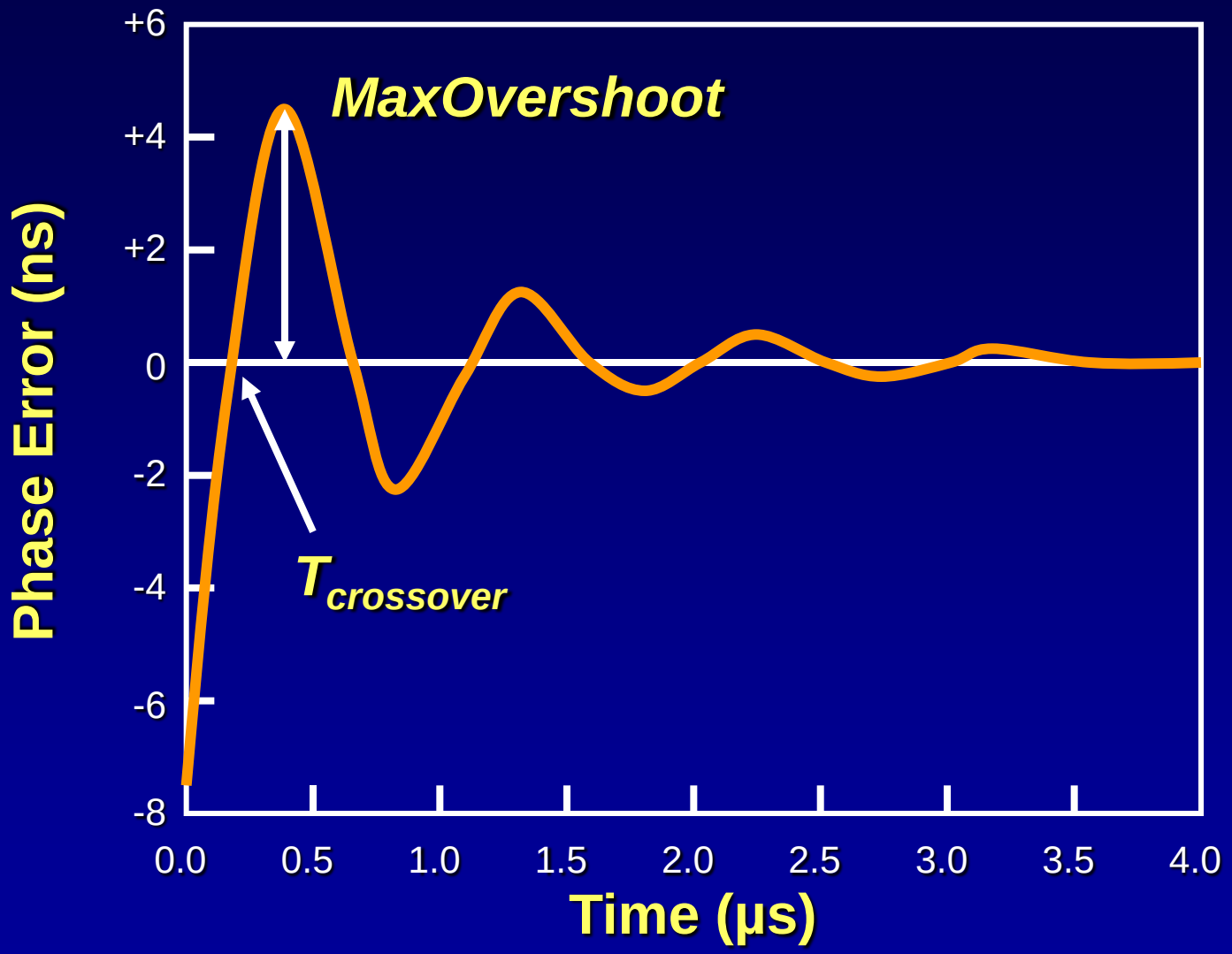
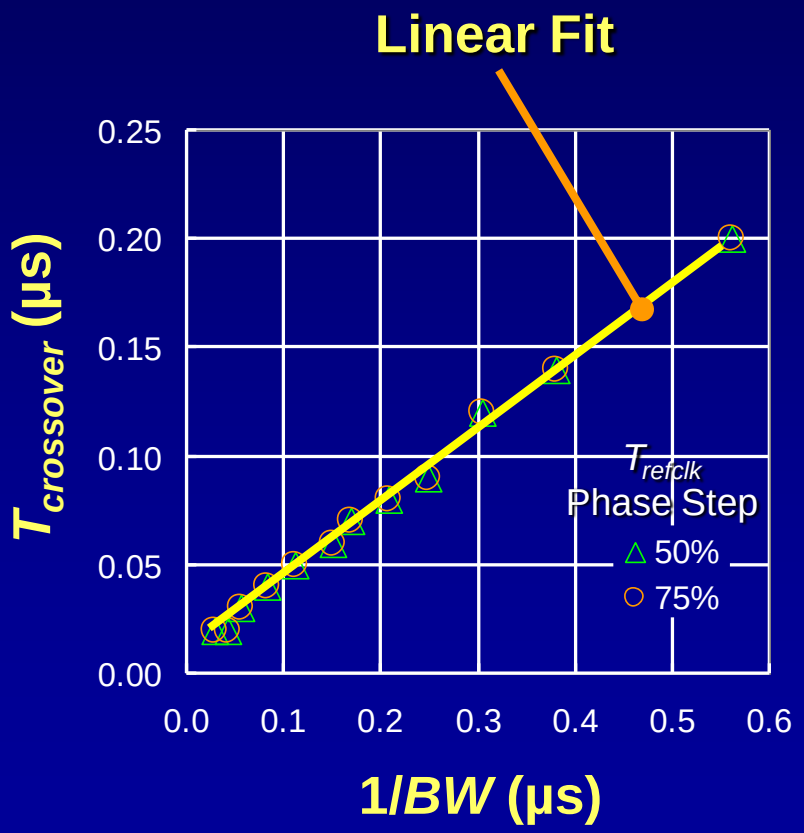
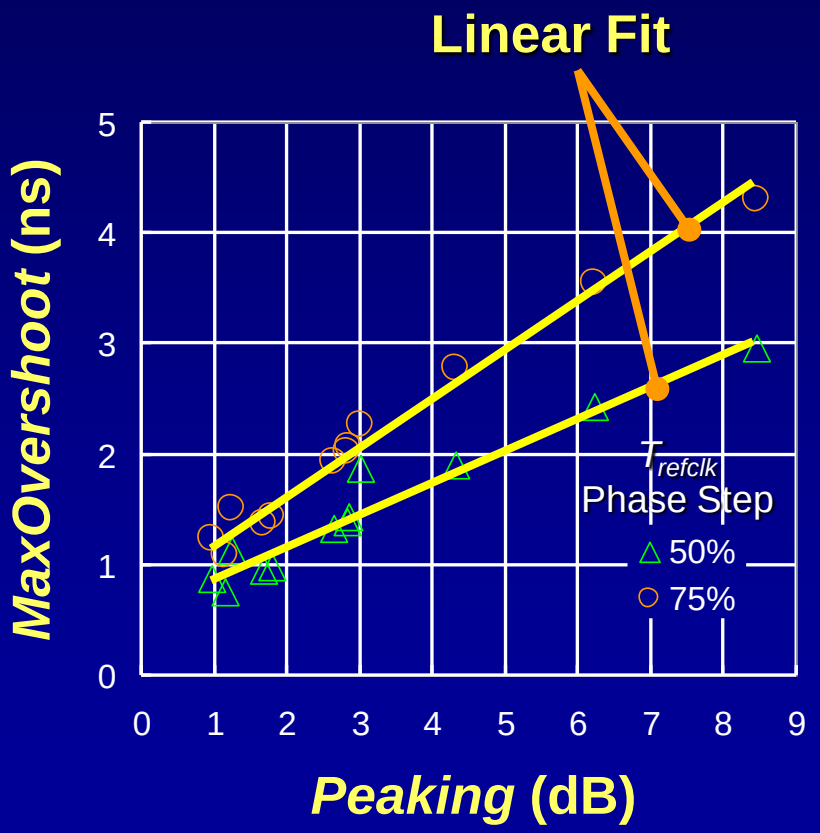
Simulated Step Response vs. Time



Basis of Algorithm

- Relationship between time & frequency domain behavior
- Lower *BW* → higher $T_{crossover}$
- Larger input phase step → larger peaking





Closed-Form Equations for Phase Error

- Damping Factor $\zeta < 1$ (underdamped)

$$\phi_{err}(t) = \phi_{step} \cdot e^{-\zeta\omega_n t} \cdot \left[\cos\left(\omega_n t \sqrt{1-\zeta^2} \right) - \frac{\zeta}{\sqrt{1-\zeta^2}} \sin\left(\omega_n t \sqrt{1-\zeta^2} \right) \right]$$

- Damping Factor $\zeta = 1$ (critically damped)

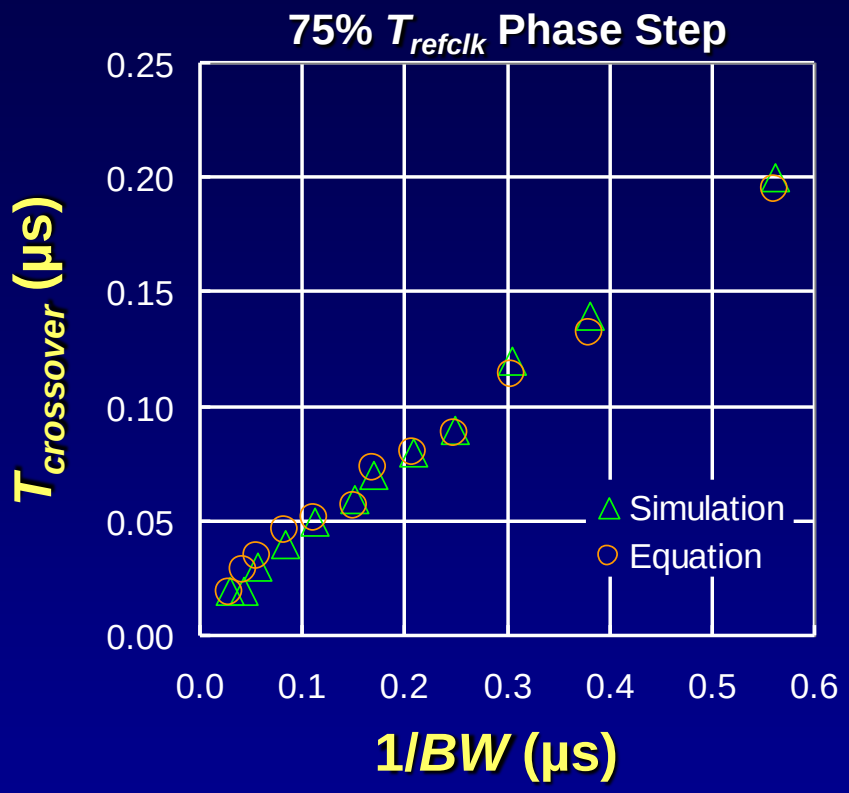
$$\phi_{err}(t) = \phi_{step} \cdot e^{-\omega_n t} \cdot (1 - \omega_n t)$$

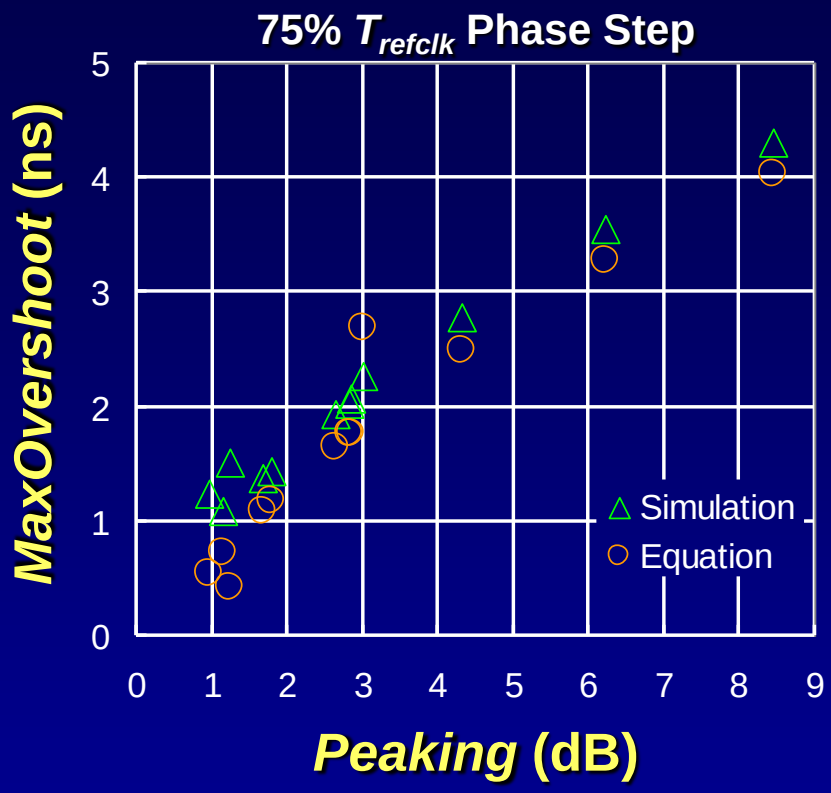
- Damping Factor $\zeta > 1$ (overdamped)

$$\phi_{err}(t) = \phi_{step} \cdot e^{-\zeta\omega_n t} \cdot \left[\cosh\left(\omega_n t \sqrt{\zeta^2 - 1} \right) - \frac{\zeta}{\sqrt{\zeta^2 - 1}} \sinh\left(\omega_n t \sqrt{\zeta^2 - 1} \right) \right]$$

Source: Gardner, *Phaselock Techniques*, 2005

Closed-Form Equations vs. Simulations

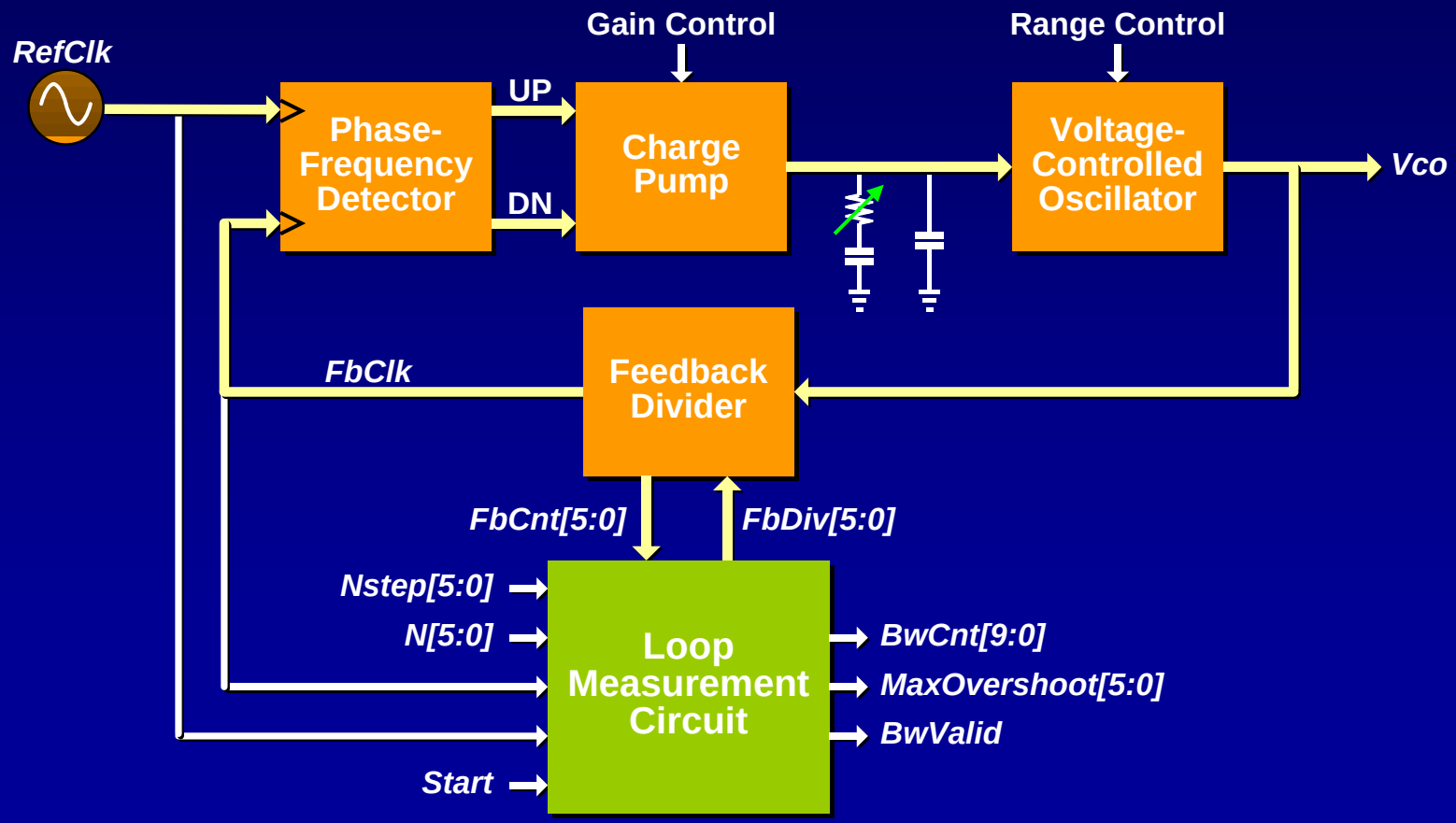




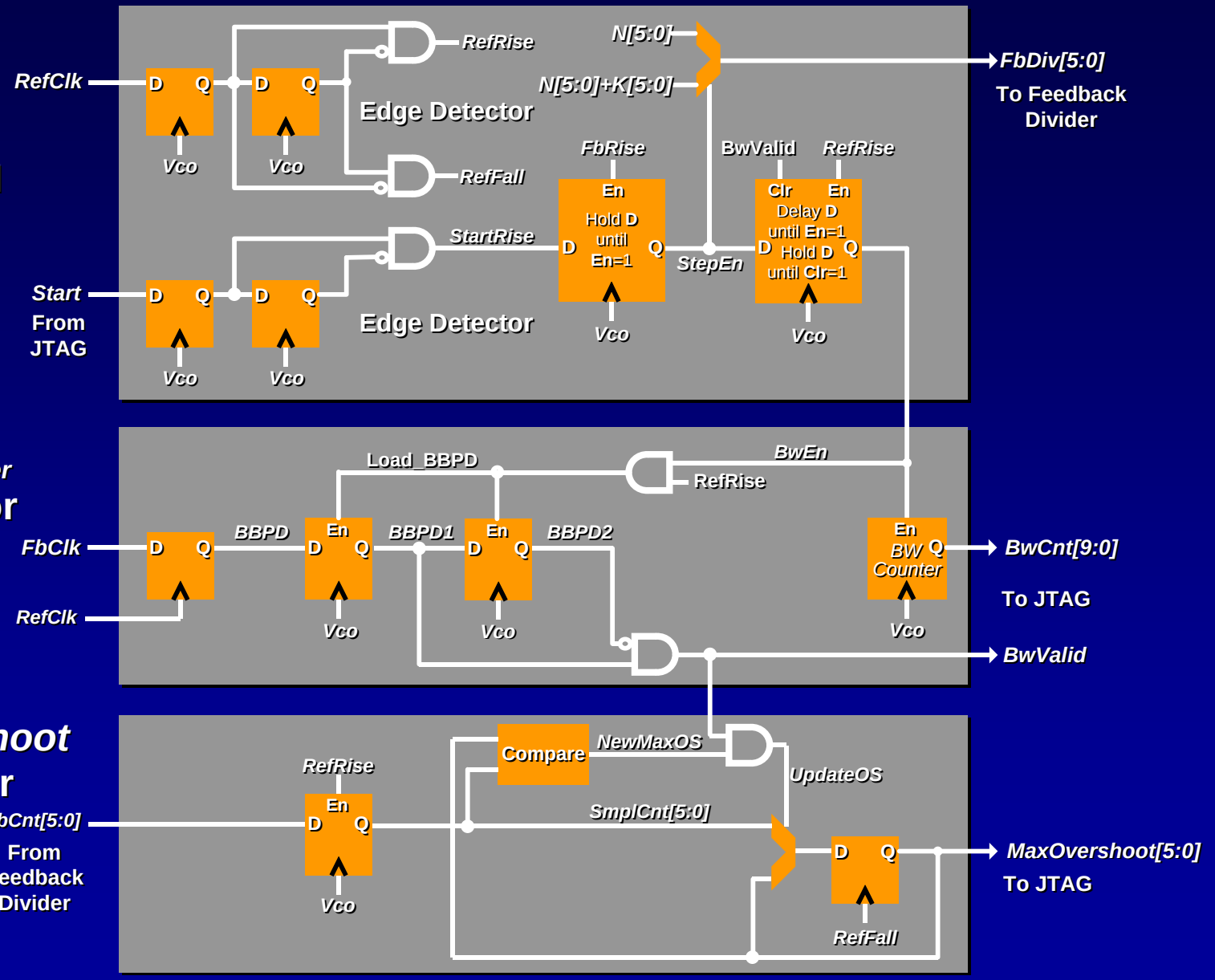
- Equations become less accurate at high ζ due to smoothing loop filter pole for reference spur reduction

PLL + Loop Measurement Circuit

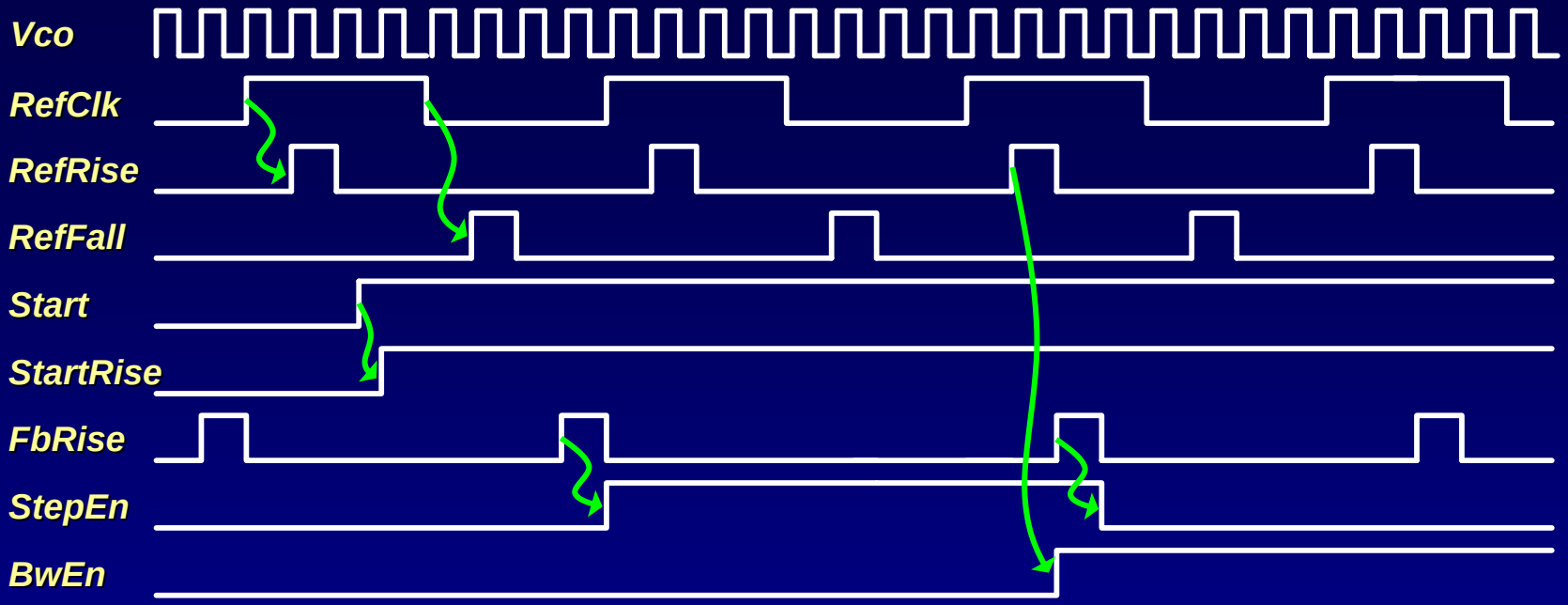
- Digital State Machine → no analog circuits
- Minimal overhead/intrusion → communicates with feedback divider only
- Instantaneously steps feedback clock phase – programmable, directional
- Measures $T_{crossover}$ and *MaxOvershoot*

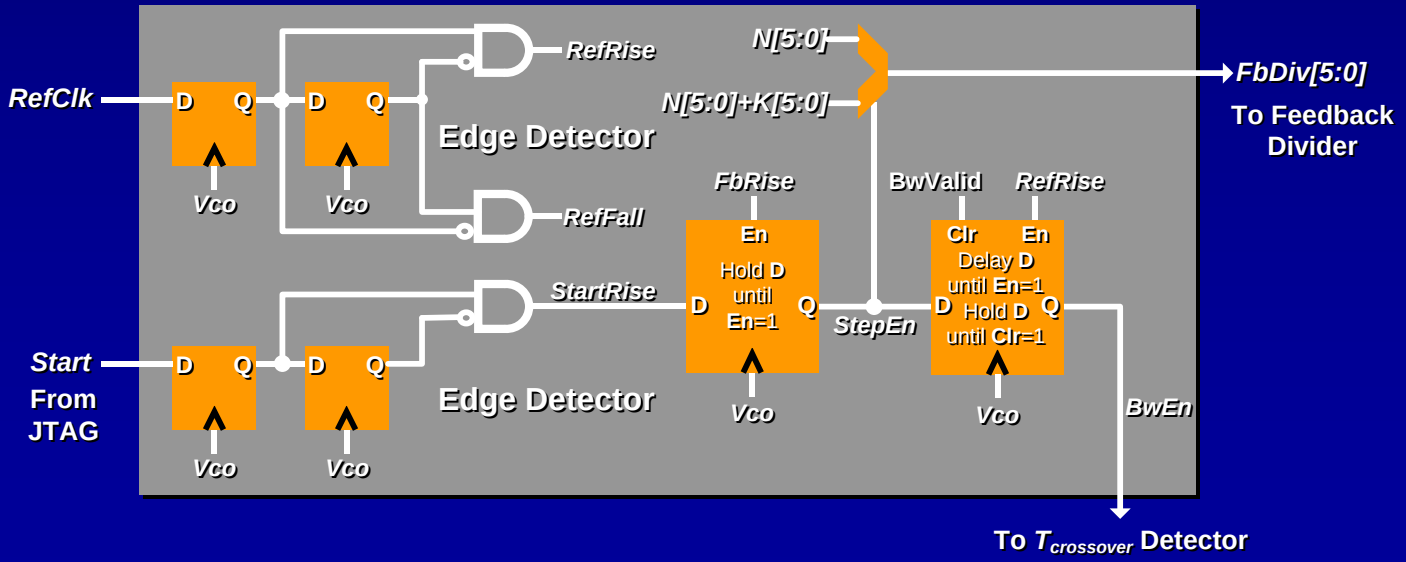


Loop Measurement Circuit

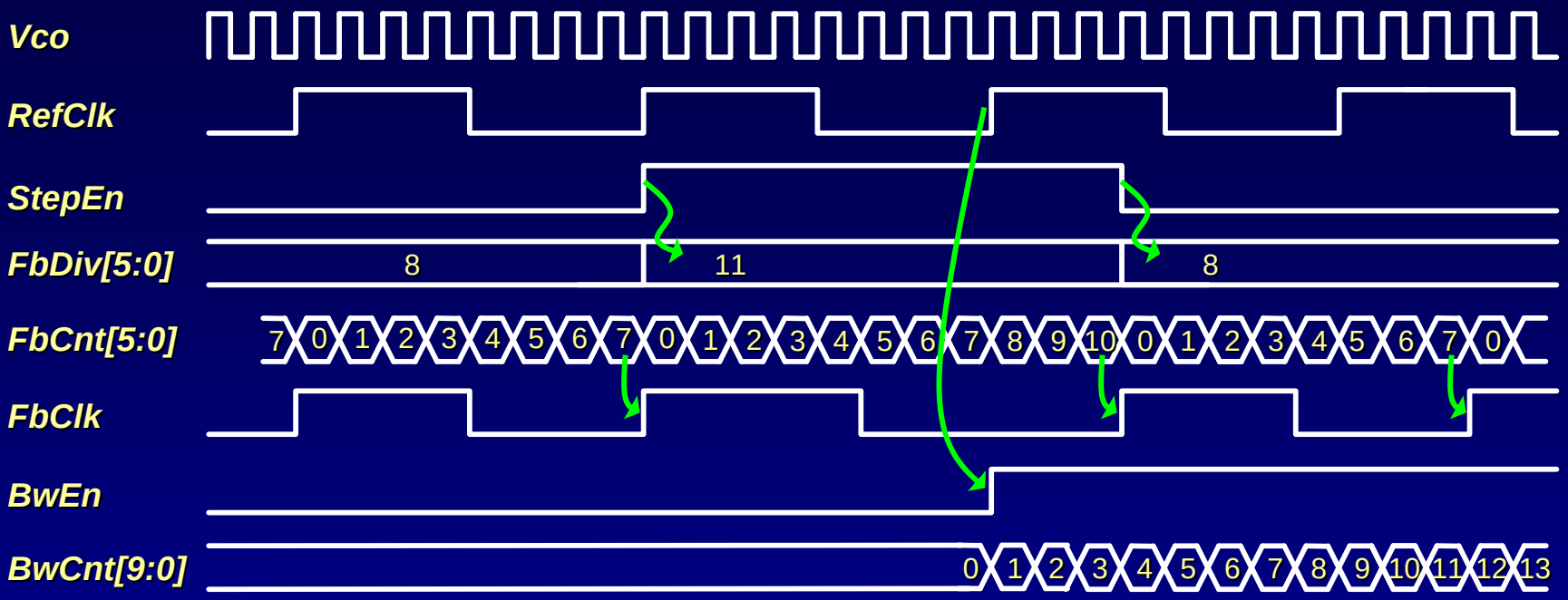


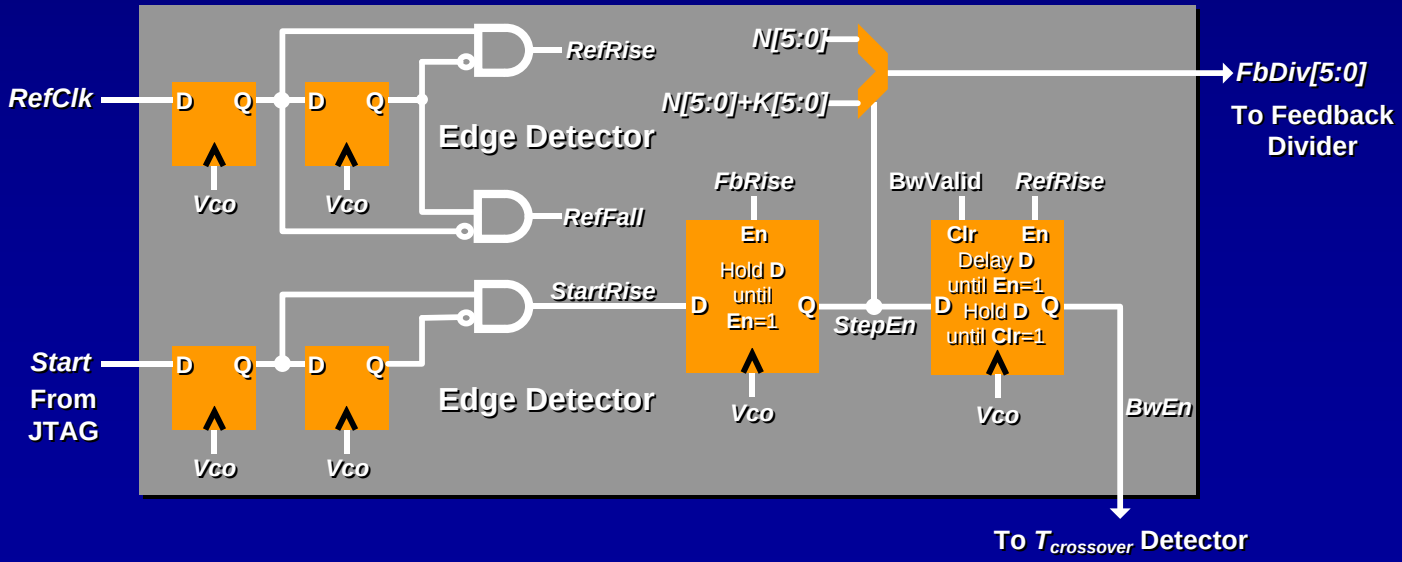
Control Unit



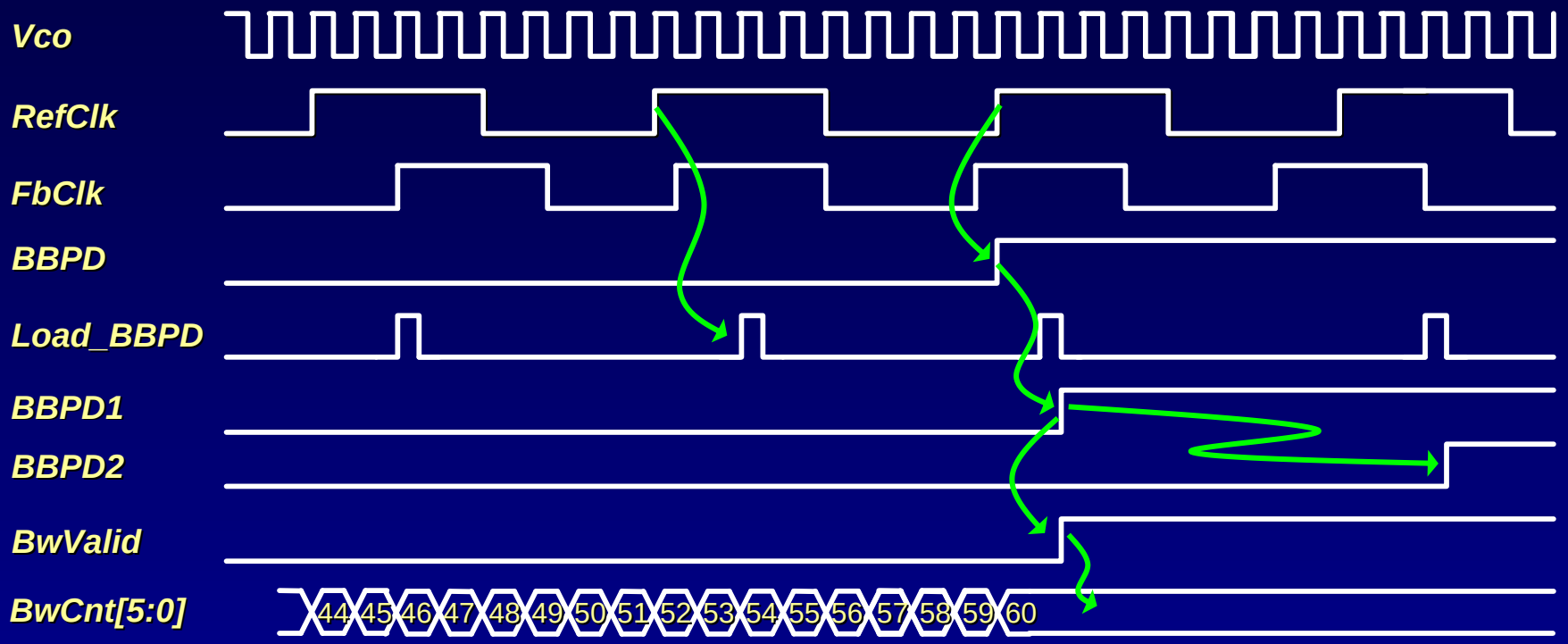


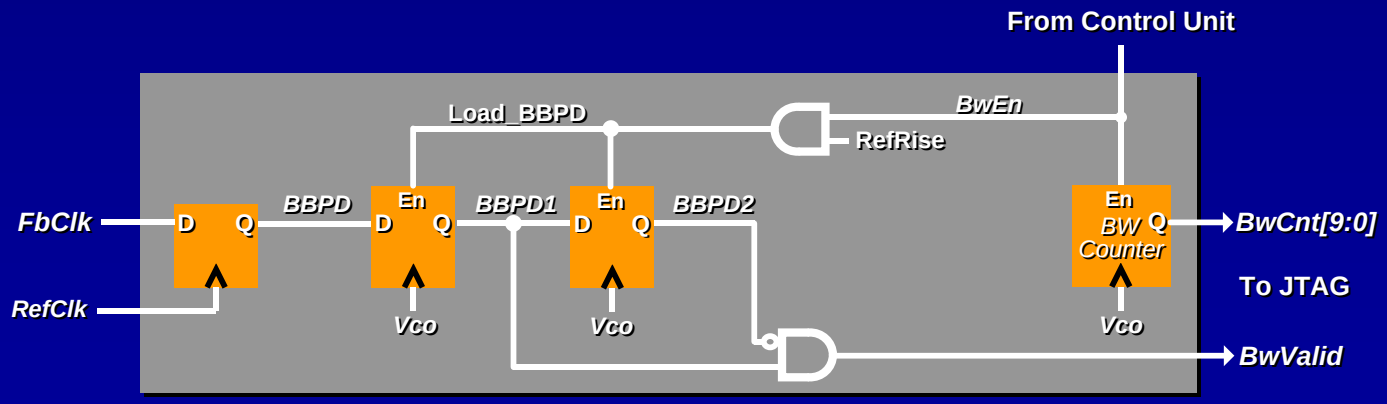
Control Unit and Phase Step



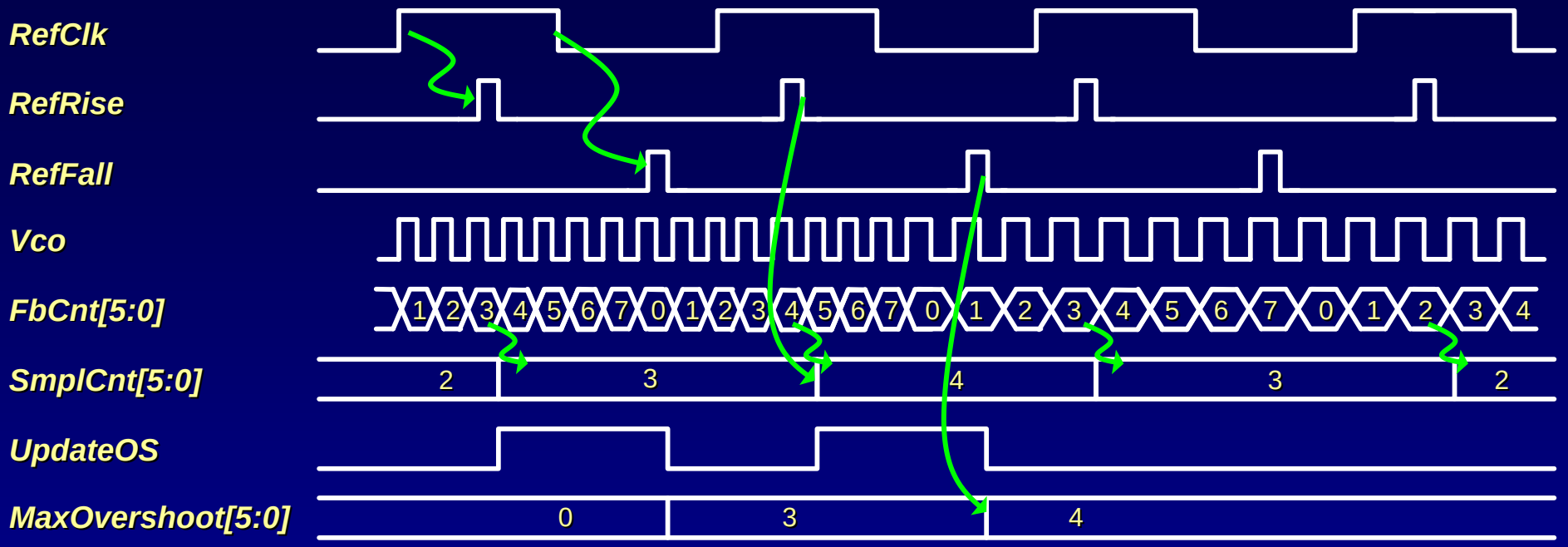


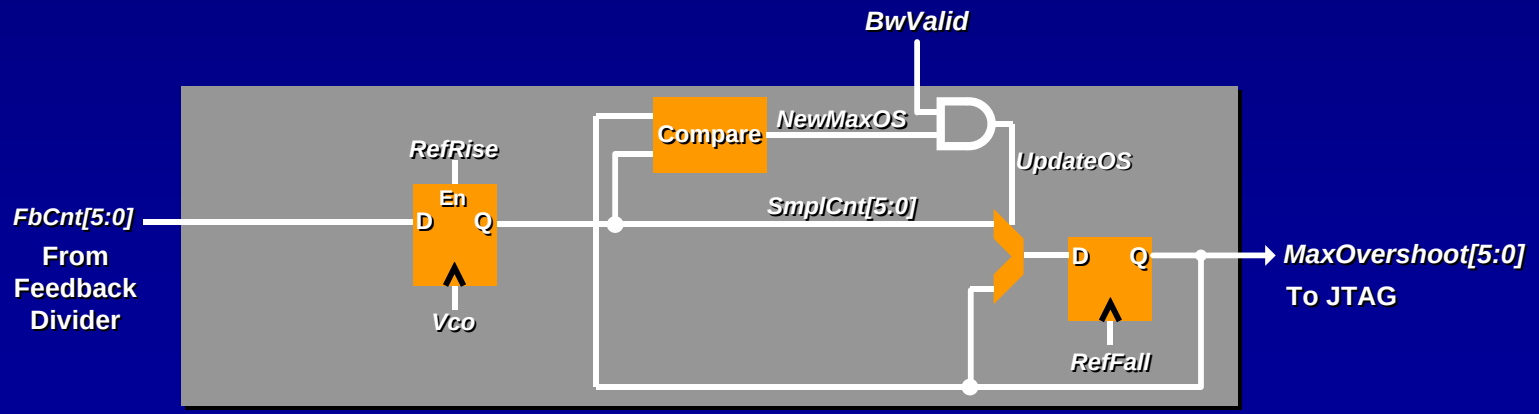
Bandwidth/Tcrossover Test





Peaking/MaxOvershoot Test





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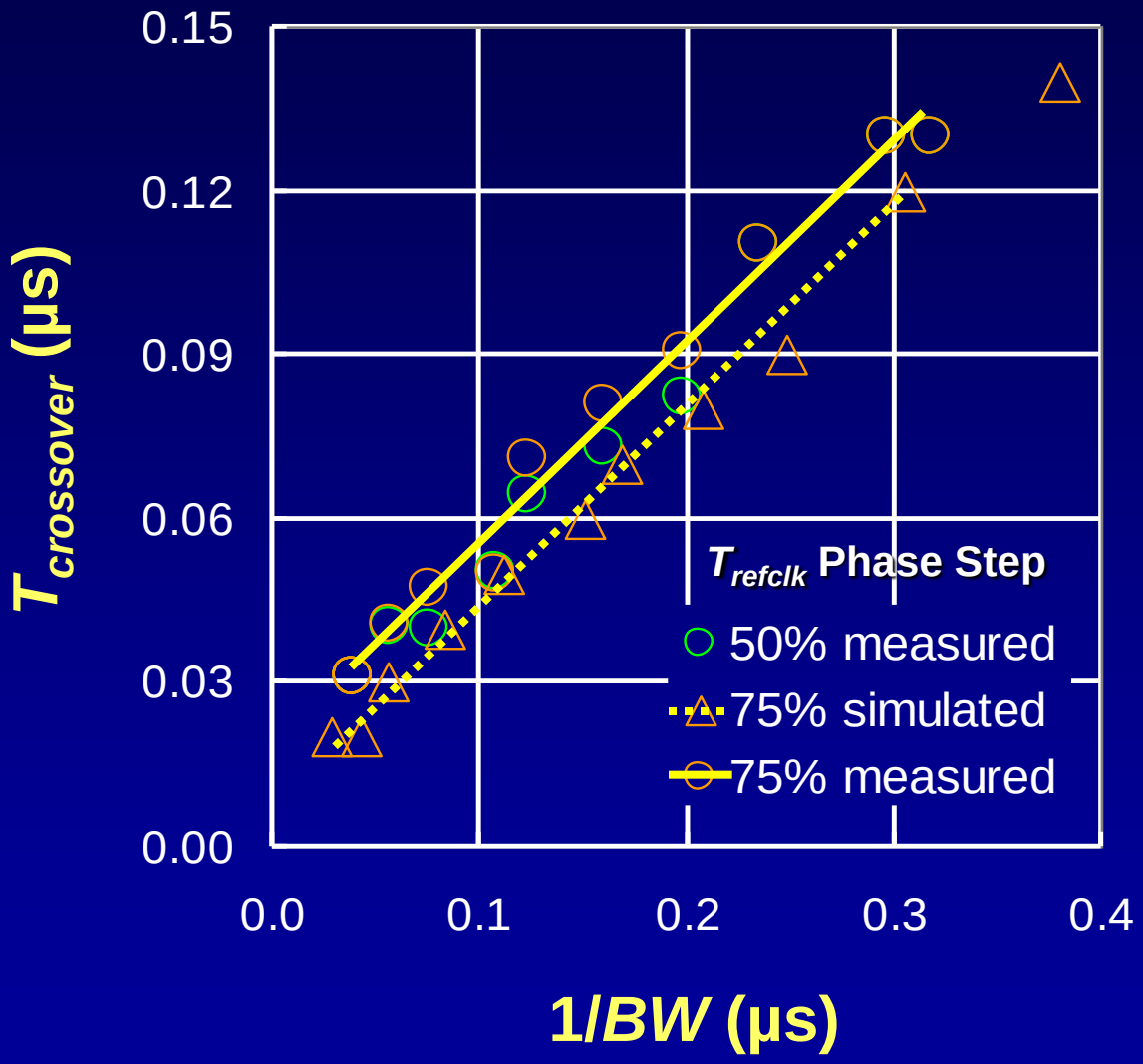
Simulations vs. Measurements

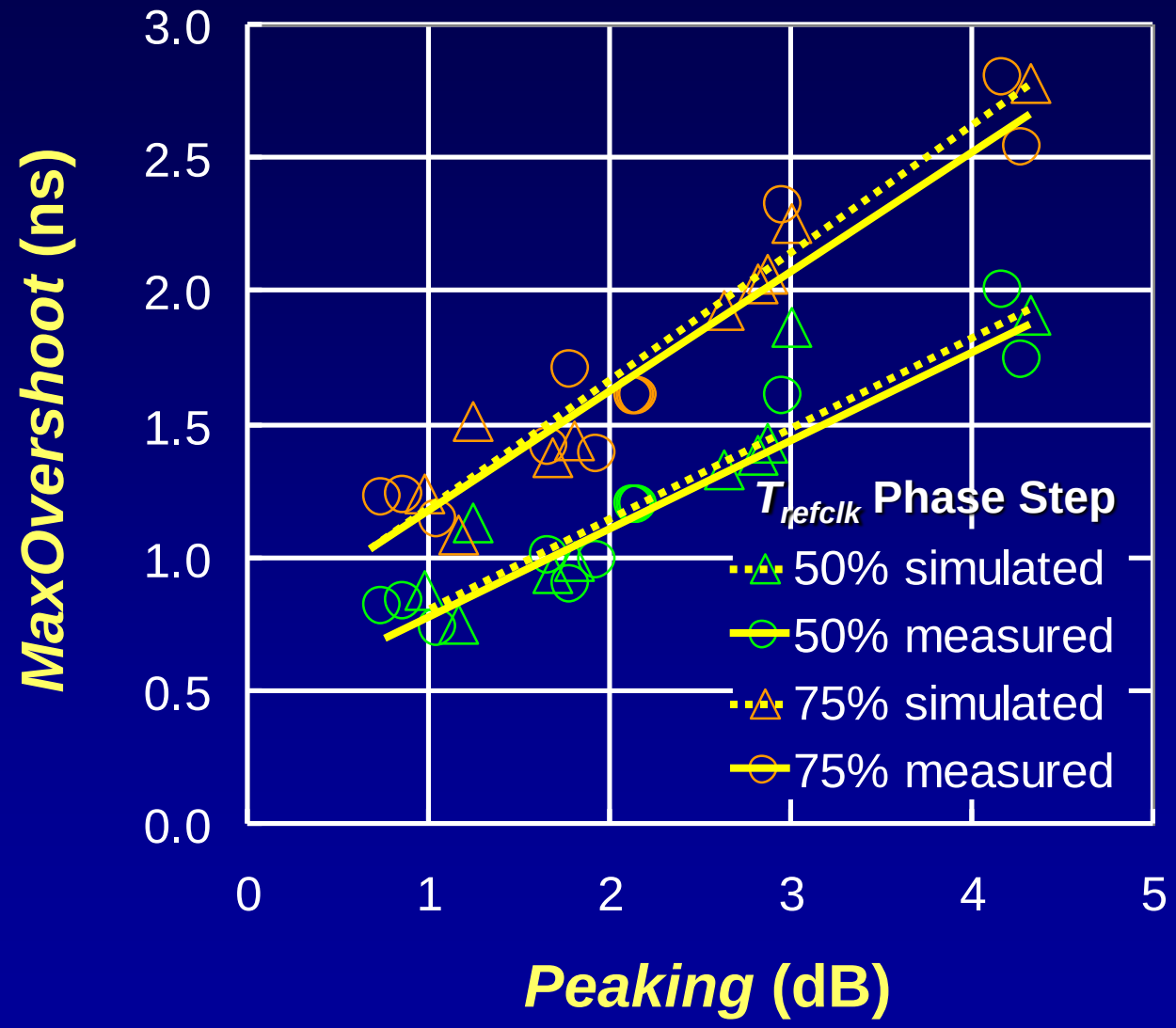
- 100 MHz refclk, feedback divisor = 50 (2x25)

Case	R_{lpf} (kΩ)	I_{cp} (μA)	Bandwidth (MHz)				Peaking (dB)			
			Simulated	Measured			Simulated	Measured		
				Part 1	Part 2	Part 3		Part 1	Part 2	Part 3
1	3.2	2.5	1.8	3.4	3.4	3.0	8.5	4.2	4.1	4.2
2	3.2	5	2.6	3.1	3.2	3.2	6.2	4.3	4.0	4.2
3	3.2	10	4.0	5.0	5.4	5.3	4.3	3.0	2.8	2.8
4	3.2	20	6.6	9.3	10.0	10.0	2.9	1.8	1.5	1.7
5	4.8	10	4.8	6.2	6.8	6.5	2.6	1.7	1.5	1.3
6	4.8	20	9.0	13.2	14.8	14.2	1.7	0.9	0.7	0.7
7	6.4	5	3.3	4.3	4.5	4.5	2.8	1.9	2.0	1.7
8	6.4	10	6.0	8.1	9.1	9.0	1.8	1.1	1.0	1.0
9	6.4	20	12.0	17.6	19.7	18.7	1.2	0.7	1.1	1.0
10	6.4	30	18.1	25.6	27.1	26.2	0.8	2.1	2.6	2.8
11	6.4	40	23.3	25.7	26.8	26.1	1.2	2.2	2.5	2.8
12	6.4	70	35.2	25.7	26.7	25.9	3.0	2.1	2.3	2.6

Measured $T_{crossover}$ vs. 1/*BW*



Measured *MaxOvershoot* vs. *Peaking*



Power and Area

- Power (simulated) = 2.5 mW
  - Output frequency = 2.5 GHz
  - *VDD* = 1.2 V
  - Clocks gated when not in use
- Area = 2,750 μm^2
  - 45-nm SOI-CMOS
  - Can easily be reduced by 40–50% by replacing non-critical sense-amplifier flip-flops with smaller master-slave flip-flops and optimizing overshoot comparator
  - Layout area not a serious concern in this design

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Conclusion

- An on-chip, all-digital state machine can be used to accurately estimate PLL bandwidth and peaking with potentially large savings in tester time.

- This flexible circuit may be used from wafer level to product level, minimizing die/package waste and allowing for adaptive PLL loop calibration.

Acknowledgments

- Alvin Loke - AMD
- Gerry Talbot - AMD